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09	CPU_DDRIIIB(NEW)	
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13	CPU_USB/LPC/SMBus(NEW)	
14	CPU_VCC_CORE(NEW)	
15	CPU_POWER(NEW)	
16	CPU_POWER_CAP1(NEW)	
17	CPU_POWER_CAP2(NEW)	
18	CPU_(VSS)(NEW)	
19	CPU_(STRAP)(NEW)	
20	LEVEL_SHIFT(NEW)	
21	DIMM_A(New)	
22	TBD	
23	DEBUG/XDP(NEW)	
24	VGA(New)	
25	TBD	
26	TBD	
27	USB_HUB(NEW)	
28	USB/USB30(New)	
29	TBD	
30	LAN_RTL8151GD	
31	AUDIO_ALC3600	
32	TBD	
33	TBD	
34	WIRELESS	
35	SATA/LED/BTN	
36	FAN_CIRCUITS/HOLE	
37	TBD	
38	SIO_ITE8732(NEW)	
39	DC_IN	
40	PWR_3P3V / 5P0V	
41	PWR_12V	
42	1D35V_0D675_TPS51363(NEW)	
43	1P5_S0&1P05_S0&1P8V_S0(NEW)	
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45	CPU_CORE&VNN(NEW)	
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47	DSW_POWER_CTL	
48	PWROK(NEW)	
49	GPU(1/5):PCI Express(NEW)	
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52	GPU(4/5):GPIO/STRAP(NEW)	
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54	GPU_DDR3_128MX16(NEW)	
55	GPU_POWER Sequence	
56	GPU_CTF/PPLAY/LDO/MVDD	
57	DC to DC_1D8V_RT8237(NEW)	
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## BOM Configuration

(R):Unmount

(G):GPU

(U):UMA

(D):Debug used

(C):HDMI Level Shift

(H):HDMI Driver IC

## PCB BOARD SIZE

6 Layers

185mm X 244mm

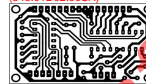
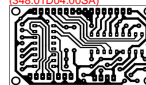
## SA BUILD

INTEL Bay Trail Platform

LAN : Gb LAN RTL8151GD

AUDIO: ALC3600

SIO\_EC:ITE8732

PCB1  
PCB  
(348.01D02.00SA)LBL1  
LABEL  
(45.3E702.001)PCB2  
PCB  
(348.01D03.00SA)LBL2  
LABEL  
(40.3EQ13.011)PCB3  
PCB  
(348.01D04.00SA)

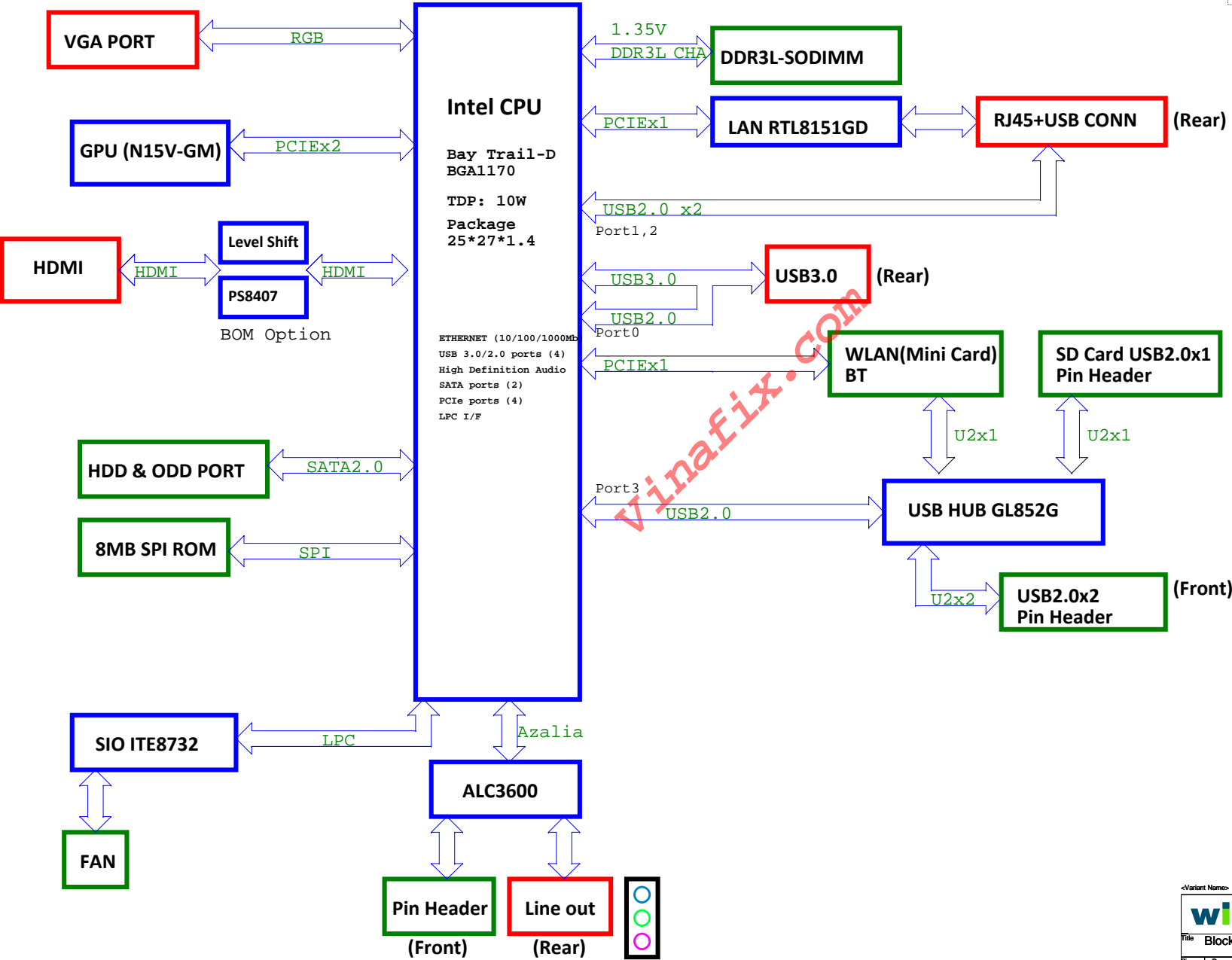
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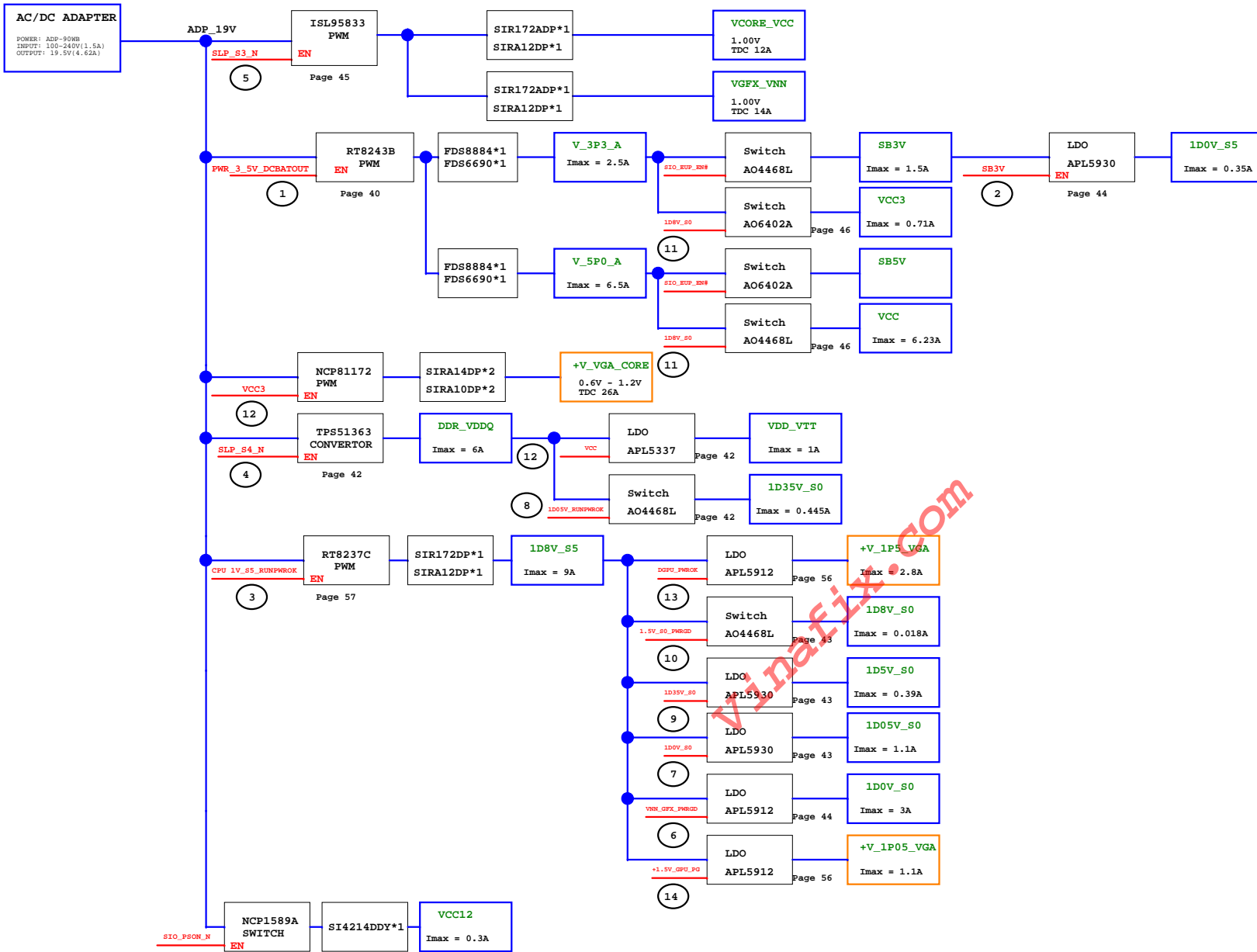
<b>wistron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Cover Page			
Size Custom	Document Number Rosa_BayTrail_DT		Rev A00
Date: Tuesday, April 15, 2014	Sheet 1 of 58		

Project Name: Saffron  
Project Code: 3PD01D010001  
PCB Version: A00  
PCB Number : 14003-1

PCB BOARD SIZE  
180mm x 244mm  
6 Layer

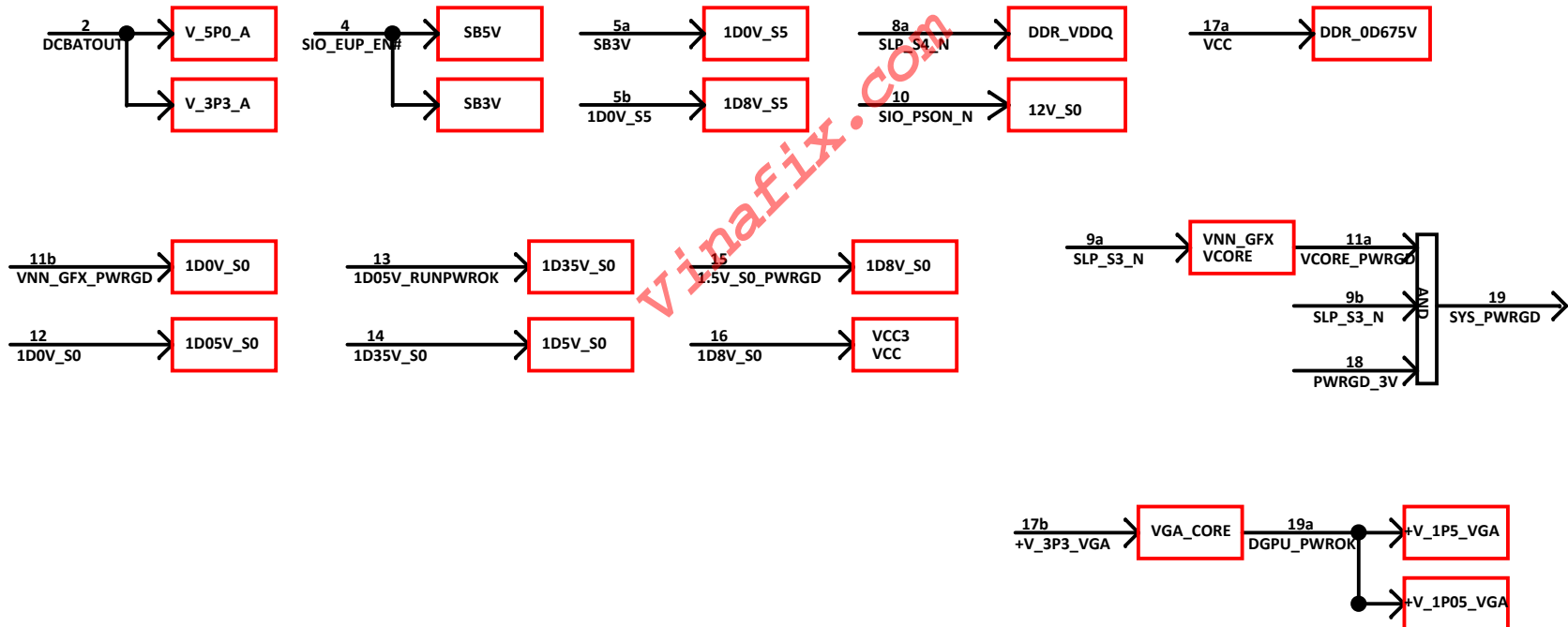
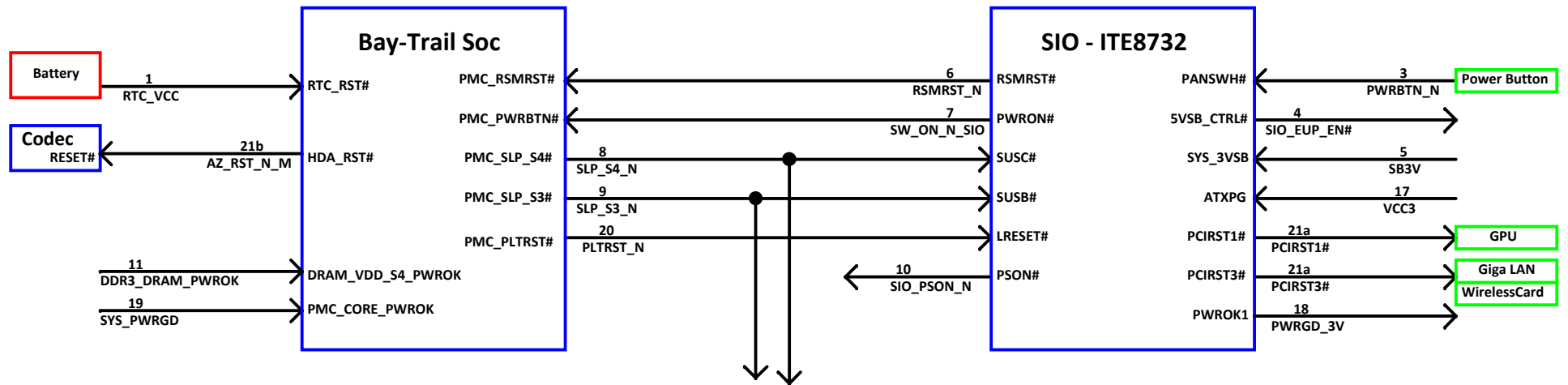
Internal Slot/Header  
Front/Rear IO  
Chipset

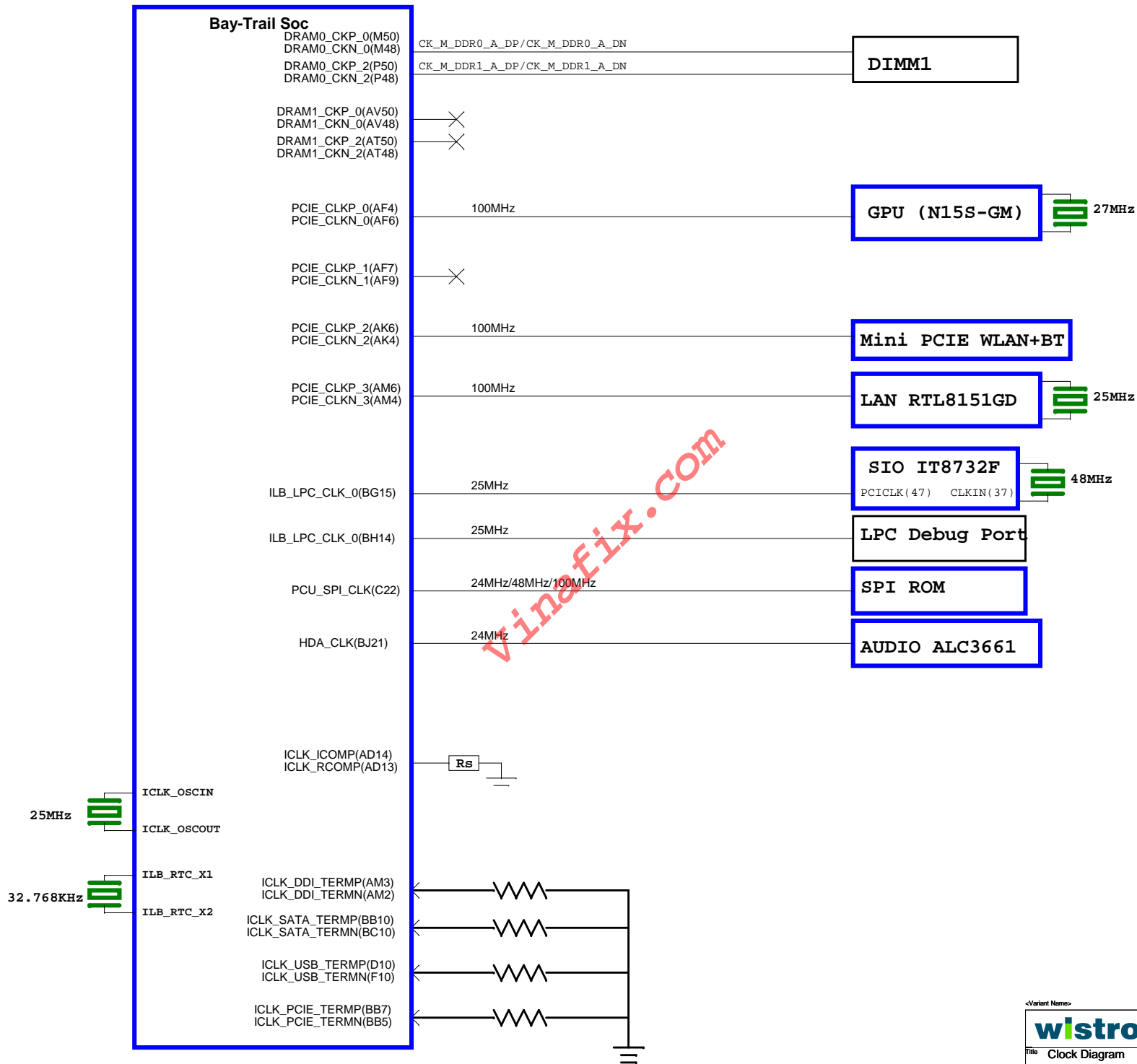




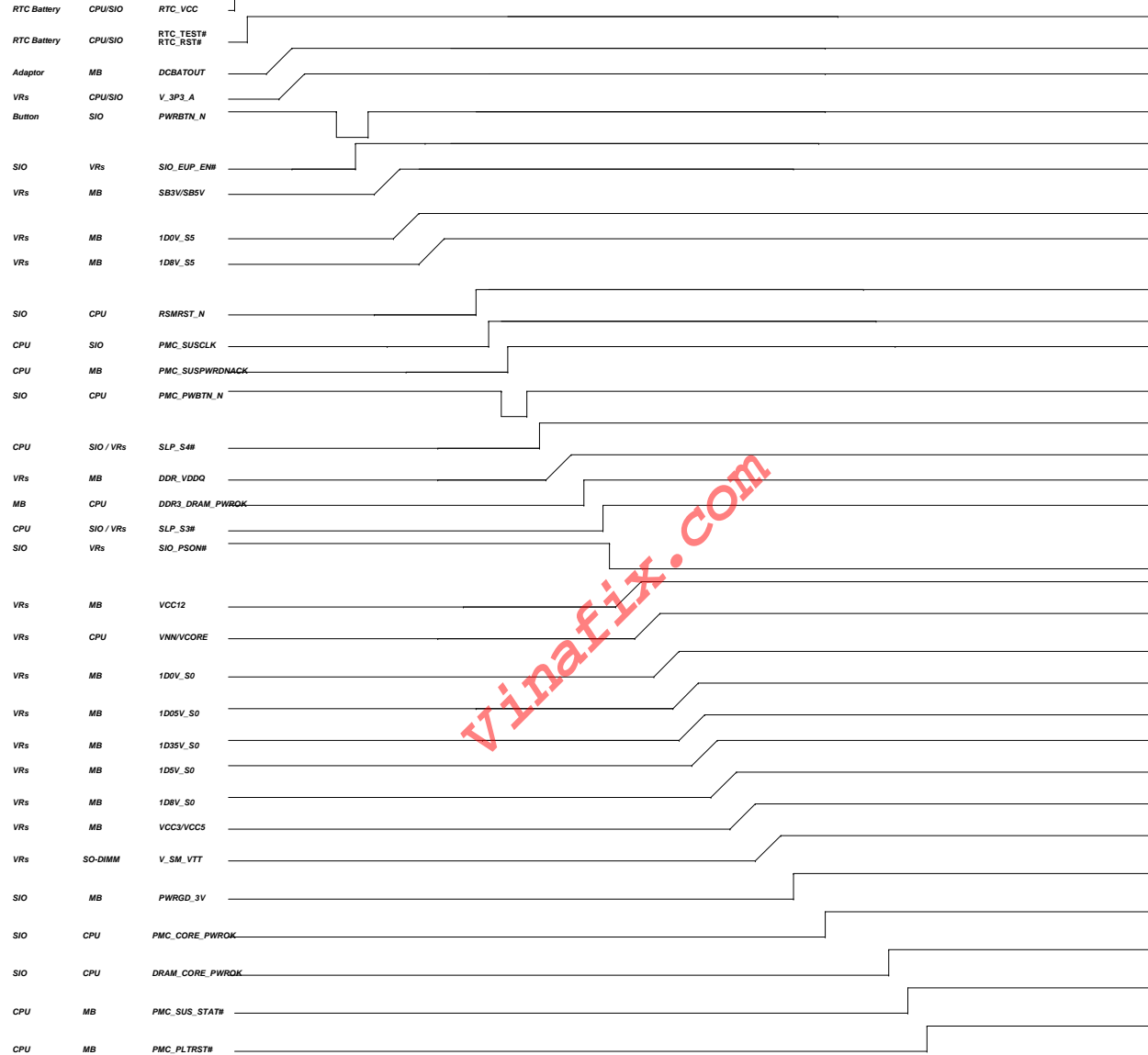
Bay Trail SoC			TDP = 10W
VCORE	VCC	0.40 ~ 1.14V ; 12A TDC	
VGFX	VNN	0.50 ~ 1.05V ; 14A TDC	
VDDQ	VDDQ	1.35V ; 1.25A	
1D0V_S5	V1P0A	1.00V ; 0.35A	
1D8V_S5	V1P8A	1.80V ; 0.065A	
V_3P3_A	V3P3A	3.30V ; 0.055A	
1D0V_S0	V1P0S	1.00V ; 3A	
1D05V_S0	V1P05S	1.05V ; 1.1A	
1P35V_S0	V1P35S	1.35V ; 0.445A	
1D8V_S0	V1P8S	1.80V ; 0.018A	
VCC3	V3P3S	3.30V ; 0.03A	
VDD_VTT	VDDQ_VTT	0.675V ; 1A	
V_3P0_BAT_VREG	VRTC	3V ; 100uA (Avg. 6uA)	

SO-DIMM	
DDR_VDDQ	V_MEM_S 1.35V ; 3.75A
VDD_VTT	V_MEM_VTT 0.675V ; 1A
SIO-IT8732	
VCC	3.3V; 20mA
V_3P3_A	3.3V; 9.37mA
BIOS ROM	
1D8V_S01	1.8V; 67mA
CPU FAN	
VCC12	12V; 300mA
USB2.0 VBUS	
VCC5_USB	5V; 500mA
VCC5_USB	5V; 900mA
LAN: RTL8151GD	
V_3P3_LAN	3.3V; 70mA
V_1P05_LAN	1.05V; 300mA (Internal Switch)
HD CODEC ALC3661-CG	
3V_VA	3.3V; 50mA
V_S_CODEC	5V; 50mA
AMP TPAS131	
19V_AMP_PVCC	19V; 270mA
DPtoLVDS_RT02136R	
DVCC33_2136	3.3V; 180mA
VNR_V12	1.2V; 210mA (Internal Switch)
Card Reader RTS5170-GR	
VCC3	3.3V; 120mA
PCI-E Mini Card	
V_3P3_PCIVDD	3.3V; 1.1A
V_1P5_PCIE	1.5V; 0.38A
WEBCAM	
VCC3_CAM	3.3V; 240mA
USB HUB - GL850-G	
HUB_VCC	5V; 52.4mA
HDD	
V_SHDD	5V; 1.1A
Slim ODD	
V_SHDD	5V; 1.5A






Source Destination Signal



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<Variant Name>

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title    TBD			
Size B	Document Number Rosa_BayTrail_DT		Rev A00
Date:	Tuesday, April 15, 2014	Sheet	7 of 58



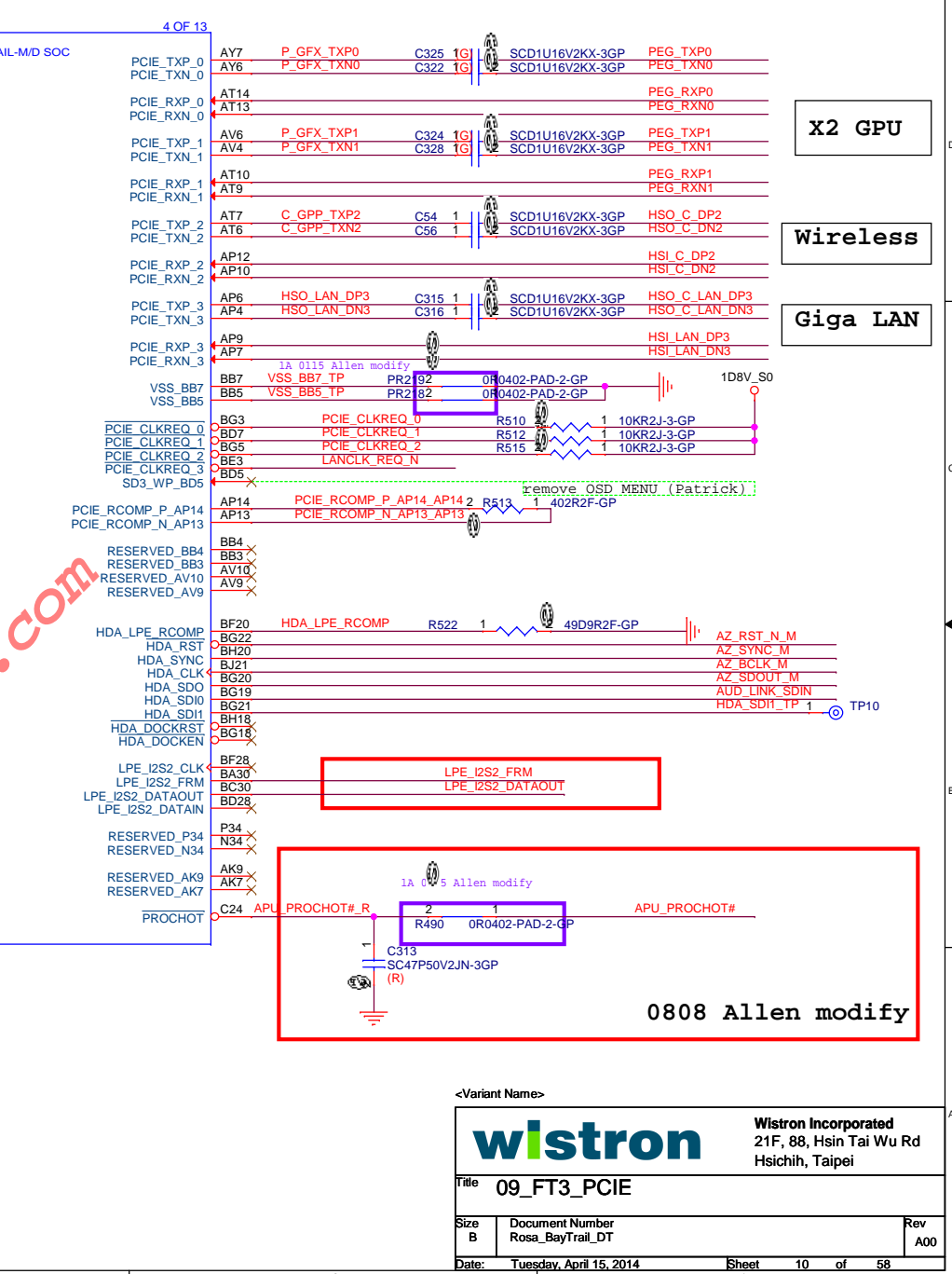
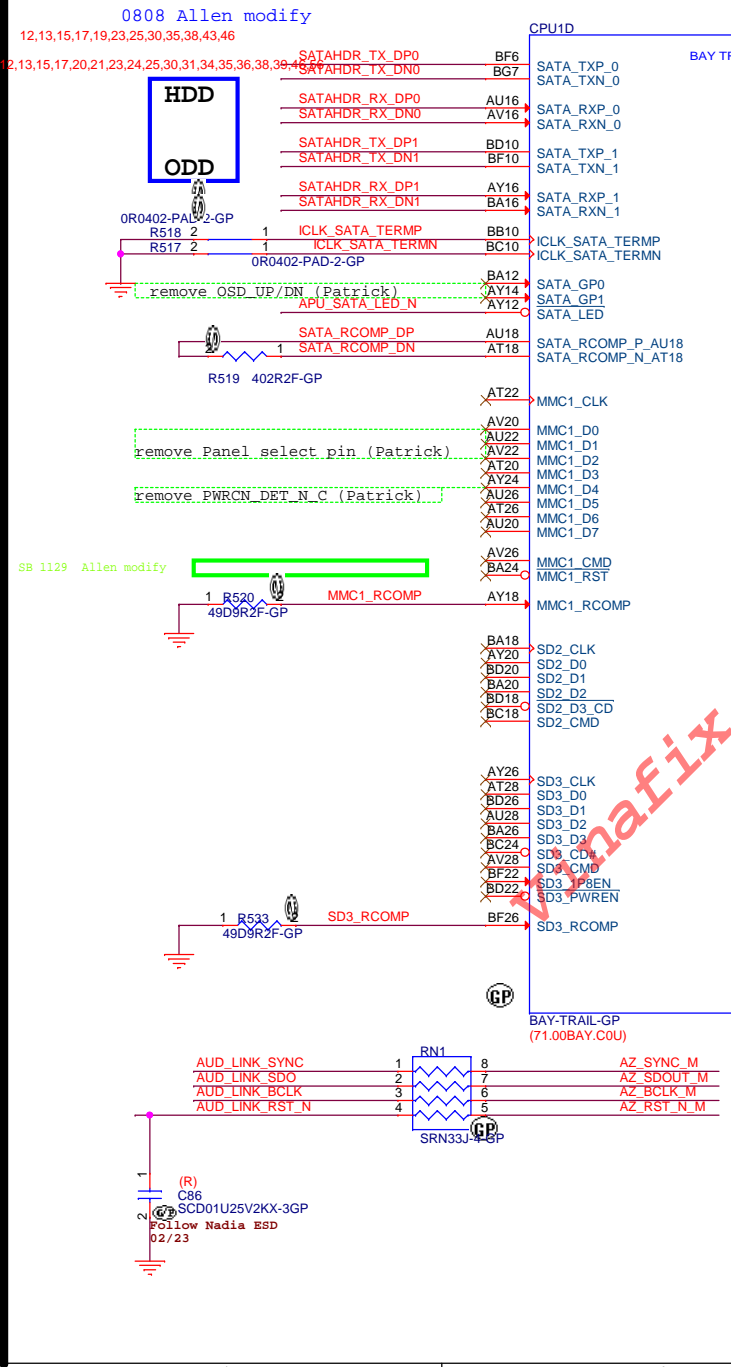
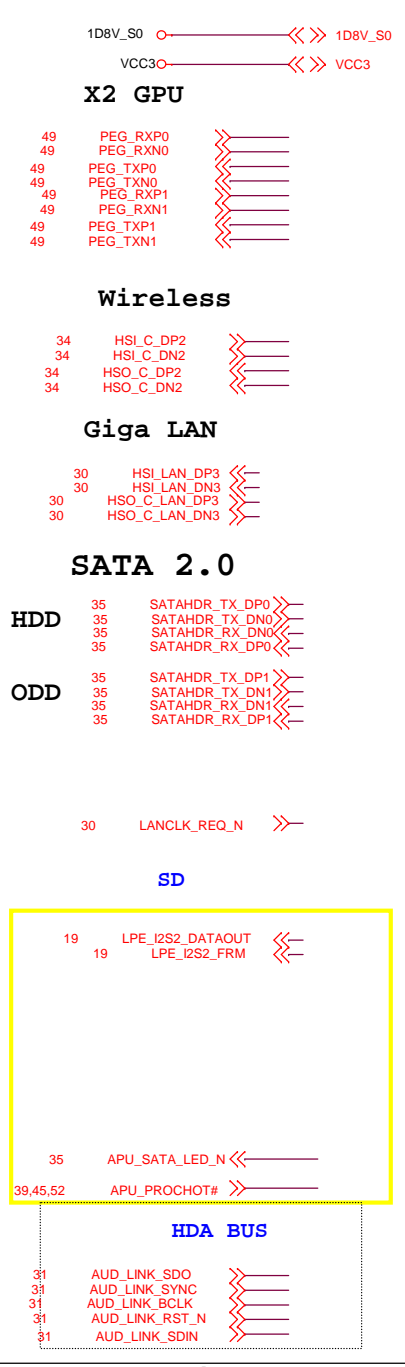


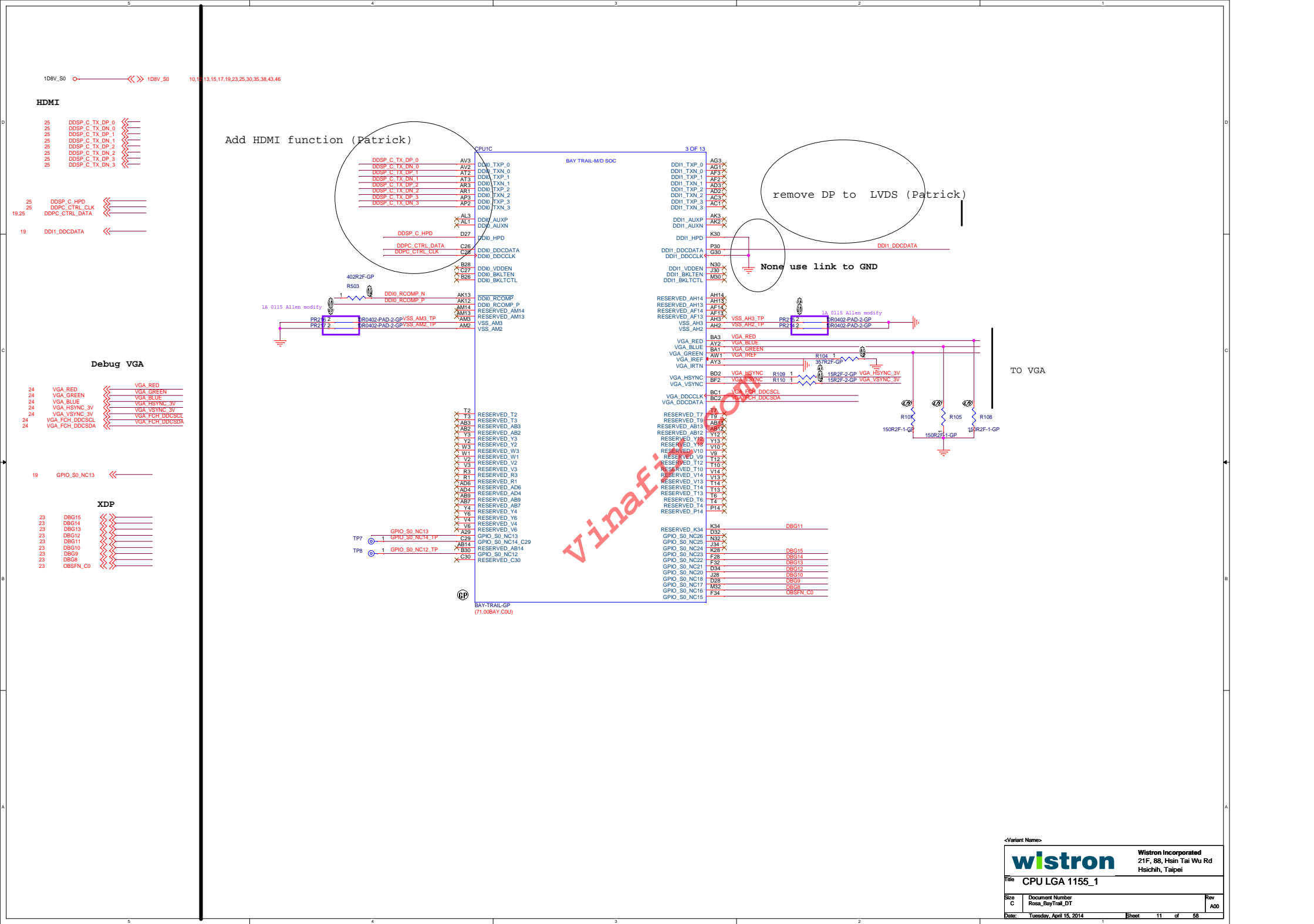
CPU1B		2 OF 13	
BAY TRAIL-MD SOC			
AY45	DRAM1_MA_0	BC38	DRAM1_DQ_0
BB47	DRAM1_MA_1	BC40	DRAM1_DQ_1
AV41	DRAM1_MA_2	BA42	DRAM1_DQ_2
BB44	DRAM1_MA_3	BC42	DRAM1_DQ_3
BB50	DRAM1_MA_4	BC38	DRAM1_DQ_4
BC53	DRAM1_MA_5	BD36	DRAM1_DQ_5
BB40	DRAM1_MA_6	BF42	DRAM1_DQ_6
BF50	DRAM1_MA_7	BC44	DRAM1_DQ_7
BC52	DRAM1_MA_8	BH40	DRAM1_DQ_8
FE52	DRAM1_MA_9	BC38	DRAM1_DQ_9
AY48	DRAM1_MA_10	BC36	DRAM1_DQ_10
BE51	DRAM1_MA_11	BJ37	DRAM1_DQ_11
BD47	DRAM1_MA_12	BU33	DRAM1_DQ_12
BA51	DRAM1_MA_13	BG37	DRAM1_DQ_13
BH49	DRAM1_MA_14	BH38	DRAM1_DQ_14
BF50	DRAM1_MA_15	AU36	DRAM1_DQ_15
X		AT36	DRAM1_DQ_16
BD38	DRAM1_DM_0	AV40	DRAM1_DQ_17
BC36	DRAM1_DM_1	AT40	DRAM1_DQ_18
BH42	DRAM1_DM_2	BA36	DRAM1_DQ_19
AT51	DRAM1_DM_3	AV36	DRAM1_DQ_20
AM42	DRAM1_DM_4	AV42	DRAM1_DQ_21
AK50	DRAM1_DM_5	AT40	DRAM1_DQ_22
AK52	DRAM1_DM_6	BJ47	DRAM1_DQ_23
X	DRAM1_DM_7	BG47	DRAM1_DQ_24
AV45	DRAM1_BAS	BJ40	DRAM1_DQ_25
AV44	DRAM1_CAS	BH46	DRAM1_DQ_26
BB51	DRAM1_WE	BG40	DRAM1_DQ_27
AY47	DRAM1_BS_0	BH40	DRAM1_DQ_28
AY44	DRAM1_BS_1	BH48	DRAM1_DQ_29
BF52	DRAM1_BS_2	BH47	DRAM1_DQ_30
X	DRAM1_BS_3	AV52	DRAM1_DQ_31
AT44	DRAM1_CS_0	AY61	DRAM1_DQ_32
AT45	DRAM1_CS_2	AP52	DRAM1_DQ_33
X		AP51	DRAM1_DQ_34
BG47	DRAM1_CKE_0	AW50	DRAM1_DQ_35
BE46	RESERVED_BE46	AW50	DRAM1_DQ_36
BD44	DRAM1_CKE_2	ARE0	DRAM1_DQ_37
BF48	RESERVED_BF48	ARE0	DRAM1_DQ_38
X		ARE3	DRAM1_DQ_39
AP41	DRAM1_ODT_0	AP47	DRAM1_DQ_40
AT42	DRAM1_ODT_2	AK53	DRAM1_DQ_41
AV50	DRAM1_CKP_0	AL41	DRAM1_DQ_42
AV48	DRAM1_CKN_0	AP48	DRAM1_DQ_43
X		AP51	DRAM1_DQ_44
AT50	DRAM1_CKP_2	AP47	DRAM1_DQ_45
AT48	DRAM1_CKN_2	AM45	DRAM1_DQ_46
X	DRAM1_DRAMRST	AM47	DRAM1_DQ_47
		AM47	DRAM1_DQ_48
		AF48	DRAM1_DQ_49
		AF50	DRAM1_DQ_50
		AM48	DRAM1_DQ_51
		AM50	DRAM1_DQ_52
		AM45	DRAM1_DQ_53
		AM45	DRAM1_DQ_54
		AL51	DRAM1_DQ_55
		AG53	DRAM1_DQ_56
		AG51	DRAM1_DQ_57
		AL53	DRAM1_DQ_58
		AK51	DRAM1_DQ_59
		AF52	DRAM1_DQ_60
		AF51	DRAM1_DQ_61
			DRAM1_DQ_62
			DRAM1_DQ_63
		BF40	DRAM1_DQSP_0
		BC36	DRAM1_DQSN_0
		BH34	DRAM1_DQSP_1
		BA36	DRAM1_DQSN_1
		AY38	DRAM1_DQSP_2
		BH44	DRAM1_DQSN_2
		BC44	DRAM1_DQSP_3
		AU53	DRAM1_DQSN_3
		AV52	DRAM1_DQSP_4
		AP42	DRAM1_DQSN_4
		AP44	DRAM1_DQSP_5
		AK47	DRAM1_DQSN_5
		AK48	DRAM1_DQSP_6
		AK53	DRAM1_DQSN_6
		AJ51	DRAM1_DQSP_7
			DRAM1_DQSN_7

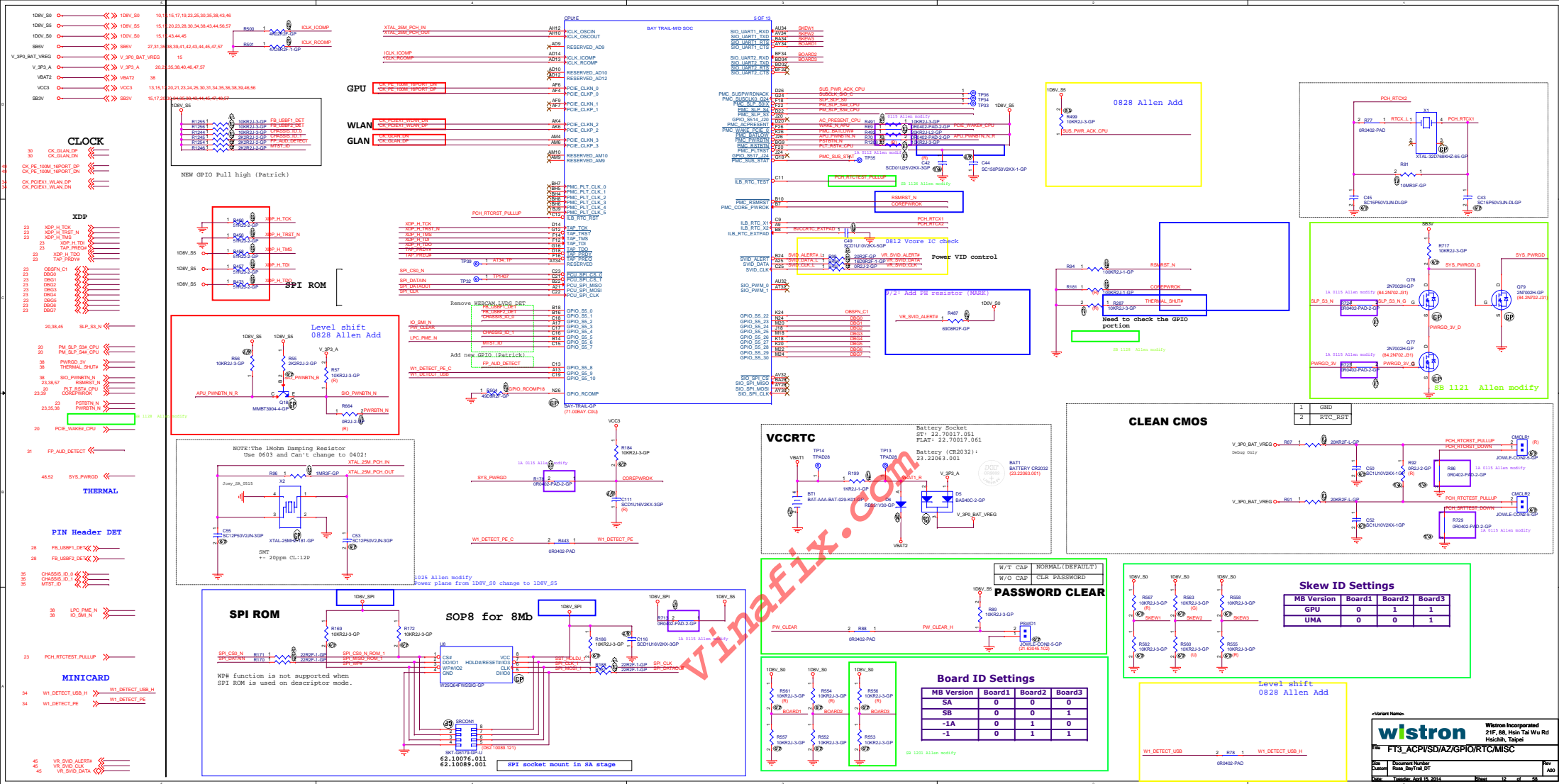
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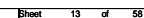
GP

BAY-TRAIL-GP  
(71.00BAY.COU)





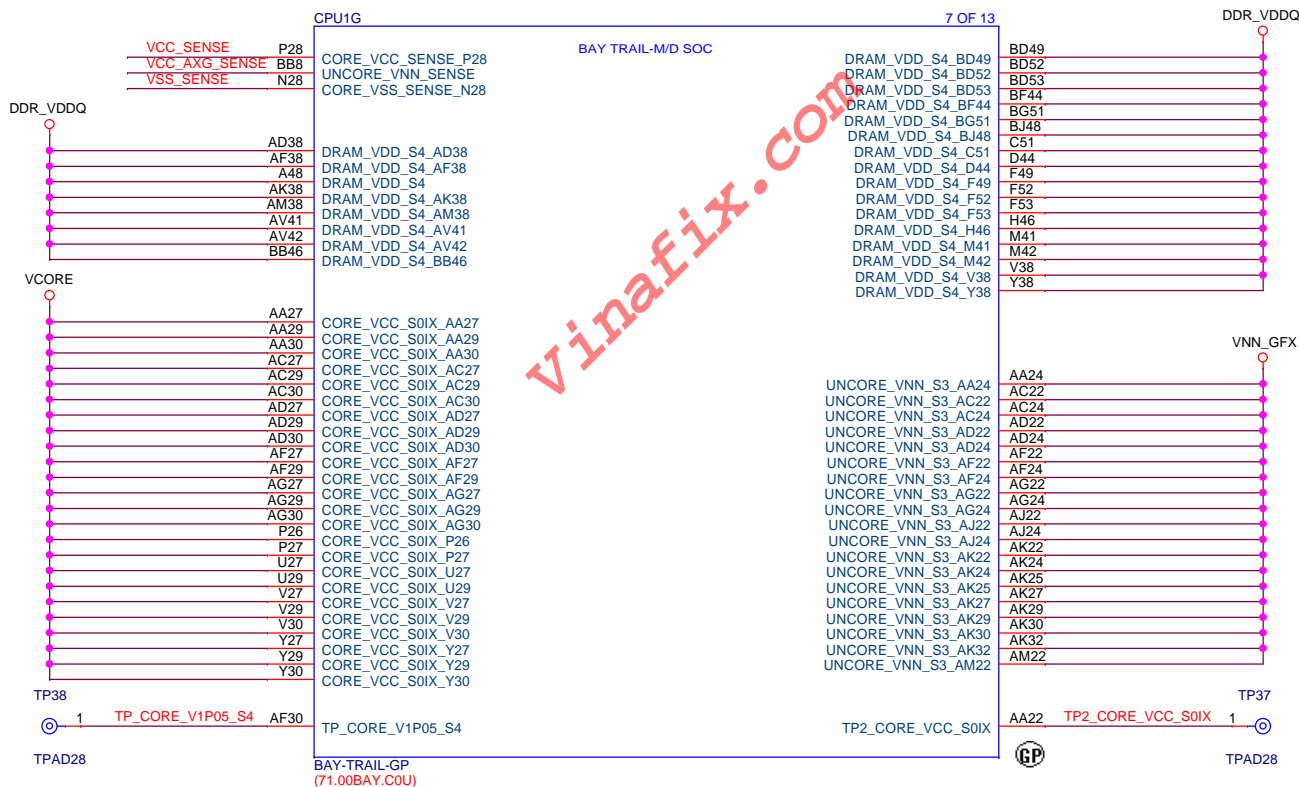
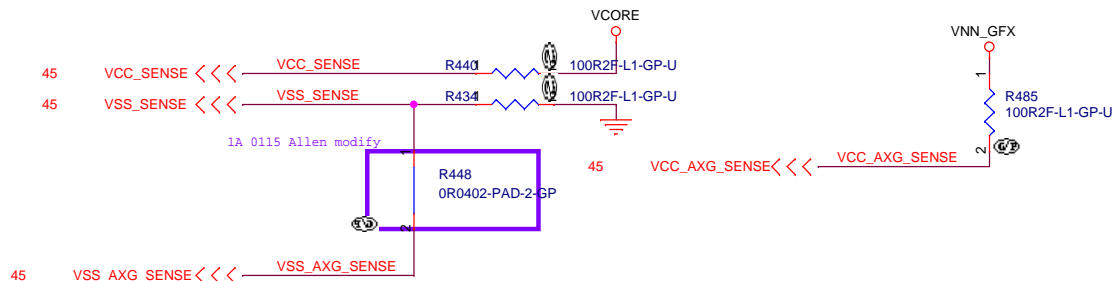




DDR\_VDDQ <<>> DDR\_VDDQ 8,16,21,42,48  
VCORE <<>> VCORE 16,38,45  
VNN\_GFX <<>> VNN\_GFX 16,45

reserve the 0402 0.1u caps on reset for EMI.

VCC_SENSE	C330	(R) 1	SCD1U10V2KX-5GP
VSS_SENSE	C284	(R) 1	SCD1U10V2KX-5GP
VSS_AXG_SENSE	C283	(R) 1	SCD1U10V2KX-5GP
VCC_AXG_SENSE	C312	(R) 1	SCD1U10V2KX-5GP



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12F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

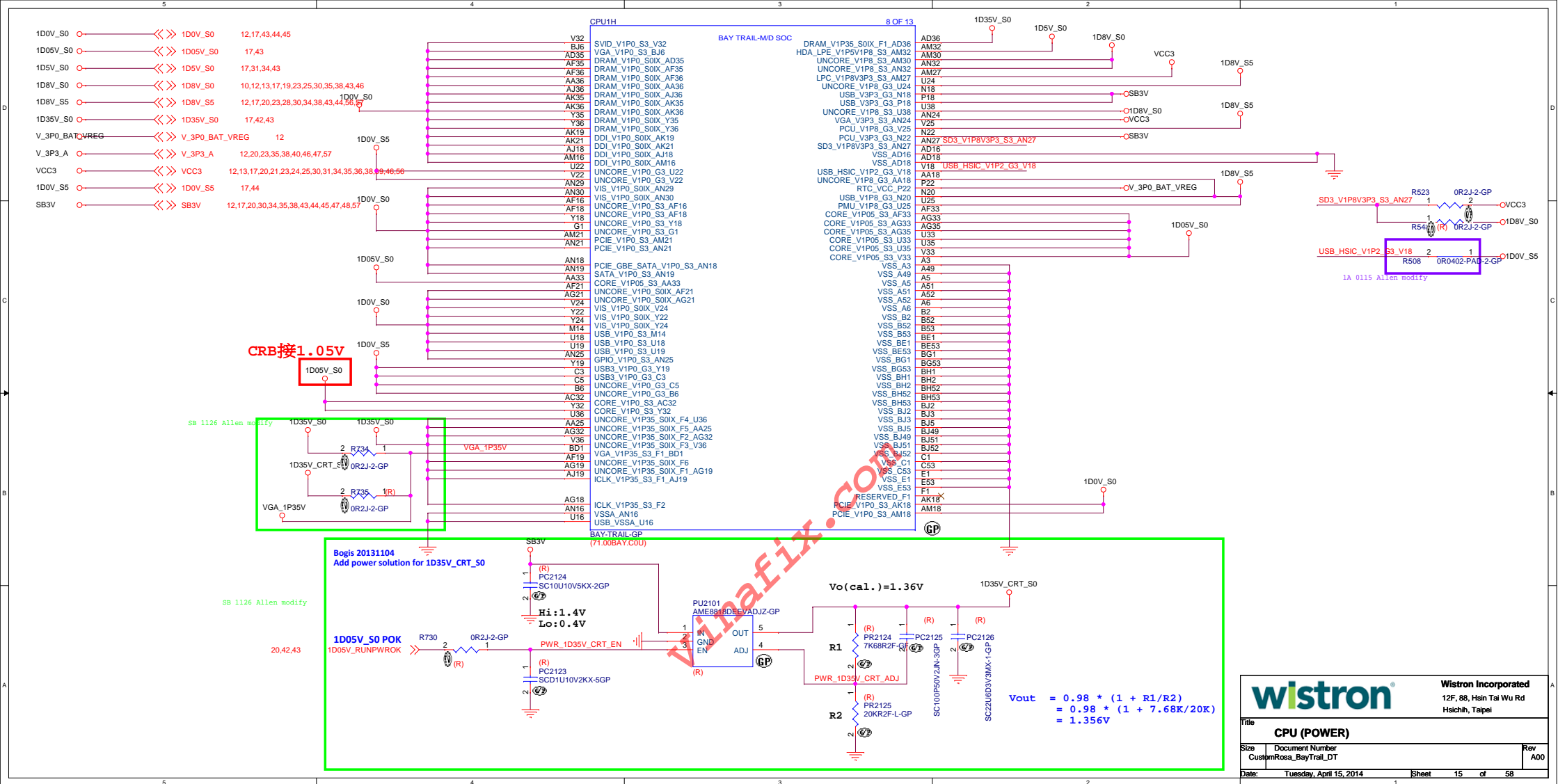
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CPU (VCC\_CORE)

Size Document Number  
Customer Rosa\_BayTrail\_DT

Rev  
A00

Date: Tuesday, April 15, 2014

Sheet 14 of 58

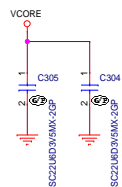


VCORE <<< VCORE 14,38,45

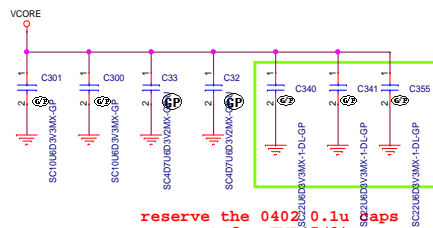
VNN\_GFX <<< VNN\_GFX 14,45

DDR\_VDDQ <<< DDR\_VDDQ 8,14,21,42,48

## VCORE

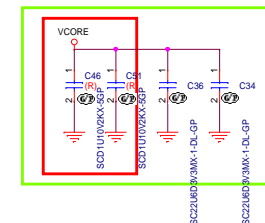


SB 1125 C340, C355 and C341 Allen modify

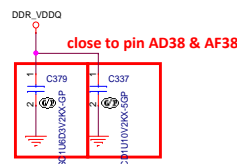
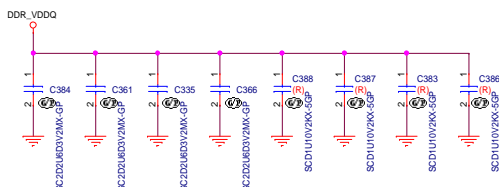


reserve the 0402 0.1u caps on reset for EMI(5/9).

SB 1128 Allen modify

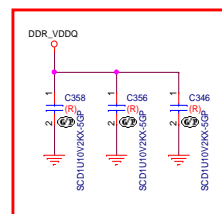


## VDDQ\_CPU

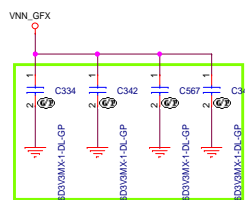
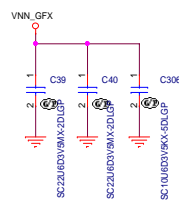
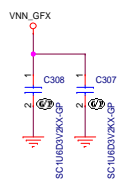


close to pin AD38 & AF38

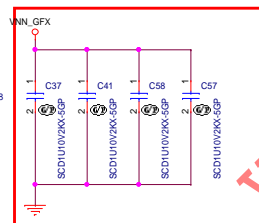
reserve the 0402 0.1u caps on reset for EMI(5/9).



## VCOREG



SB 1120 C334, C342, C348, C567 Allen modify

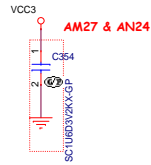


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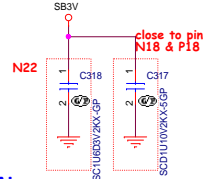


1D0V_S0	100V_S0	12,15,43,44,45
1D0V_S5	100V_S5	15,44
1D05V_S0	1005V_S0	15,43
1D5V_S0	105V_S0	15,31,34,43
1D8V_S0	108V_S0	10,12,13,15,19,23,25,30,35,38,43,46
1D8V_S5	108V_S5	12,15,20,23,28,30,34,38,43,44,56,57
1D35V_S0	1035V_S0	15,42,43
V_3P3_A	V_3P3_A	12,20,23,35,38,40,46,47,57
VCC3	VCC3	12,13,15,20,21,23,24,25,30,31,34,35,36,38,39,46,56
SB3V	SB3V	12,15,20,30,34,35,38,43,44,45,47,48,57

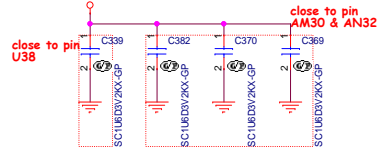
### +3P3V\_MAIN



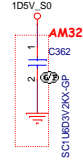
### +3P3V\_AUX



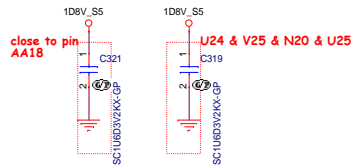
### 1D8V\_S0



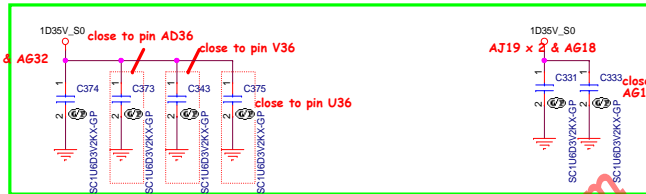
### 1D5V\_S0



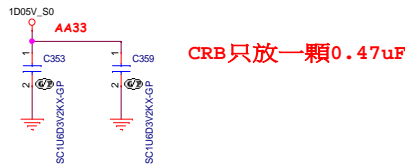
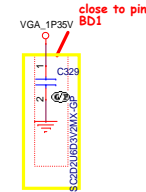
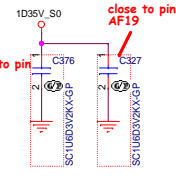
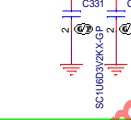
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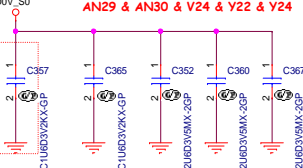
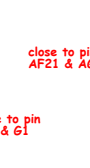
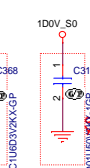
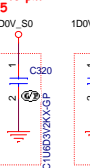
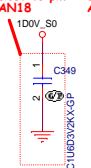
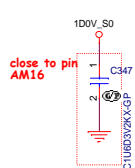
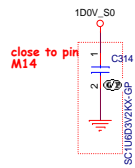
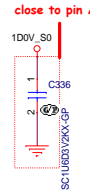
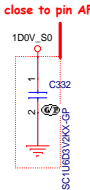
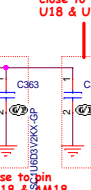
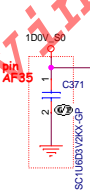
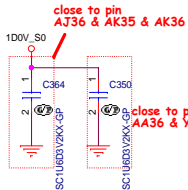
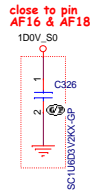
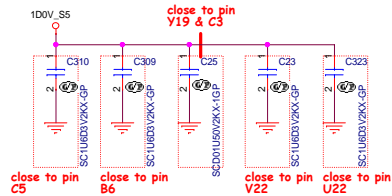
SB 1128 Allen modify

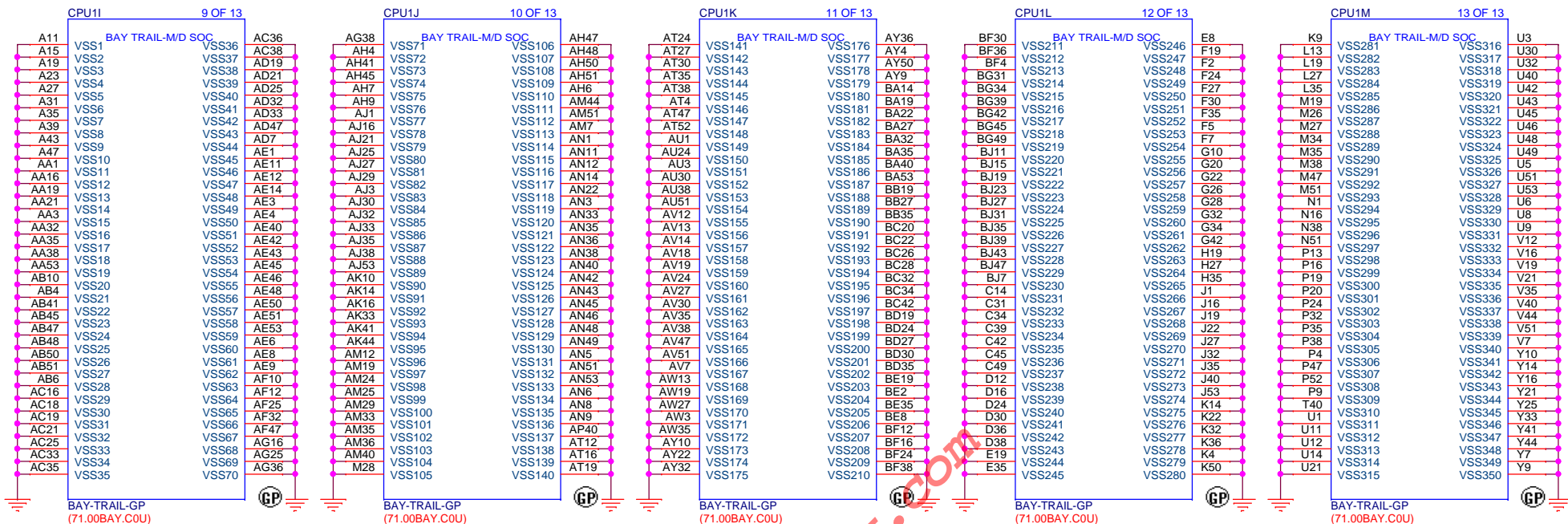


### 1D35V\_S0



CRB只放一顆0.47uF





Wistron Incorporated  
12F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title  
**CPU (VSS)**

Size Document Number  
CustomRosa\_BayTrail\_DT

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A00

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STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDIO Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDIO_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
<b>Schematic</b>						
<b>High</b>	SPI	Normal Operation	DDIO detected	DDI1 detected	DDI1 detected	
<b>Low</b>	LPC	Override	DDIO not detected	DDI1 not detected	DDI1 not detected	

## 2.25 Hardware Straps

All straps are sampled on the rising edge of PMC\_CORE\_PWROK.

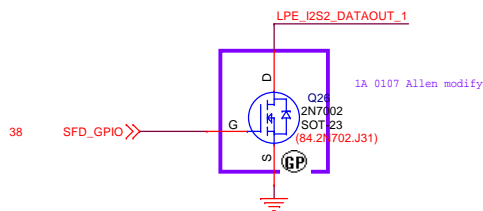
Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDIO_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDIO Detect 0 = DDIO not detected 1 = DDIO detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

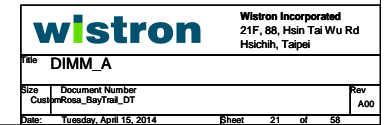
### 27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

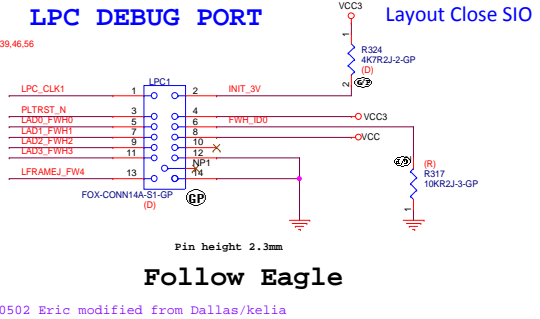
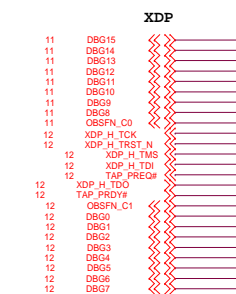
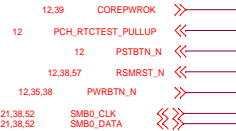
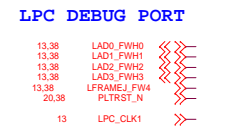
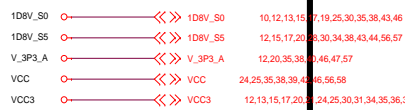
**Note:** The Top-Swap strap is an active high signal and is multiplexed with the GPIO\_S0\_SC[56] signal.







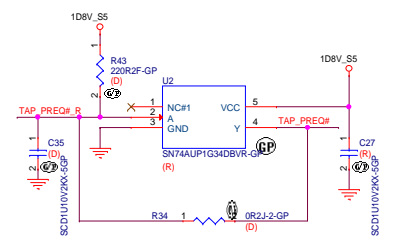
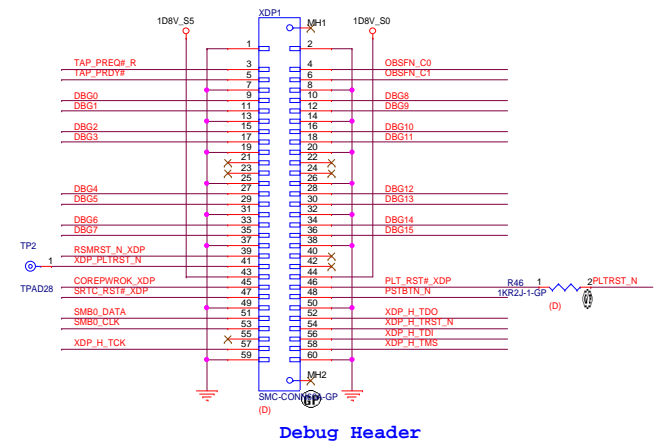
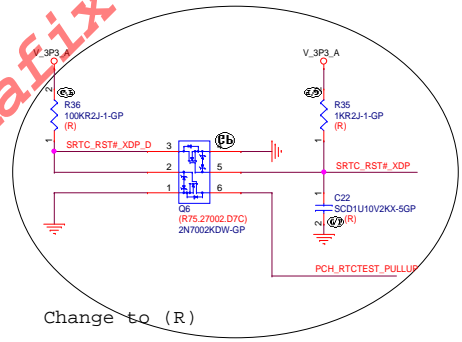
Vinafix.com



Follow Eagle

0502 Eric modified from Dallas/kelia

Vinafix.com







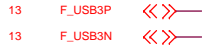


Remove DP to LVDS CIRCUIT

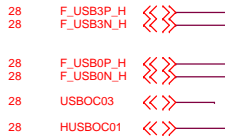
[vinafix.com](http://vinafix.com)



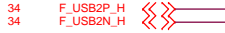
From CPU



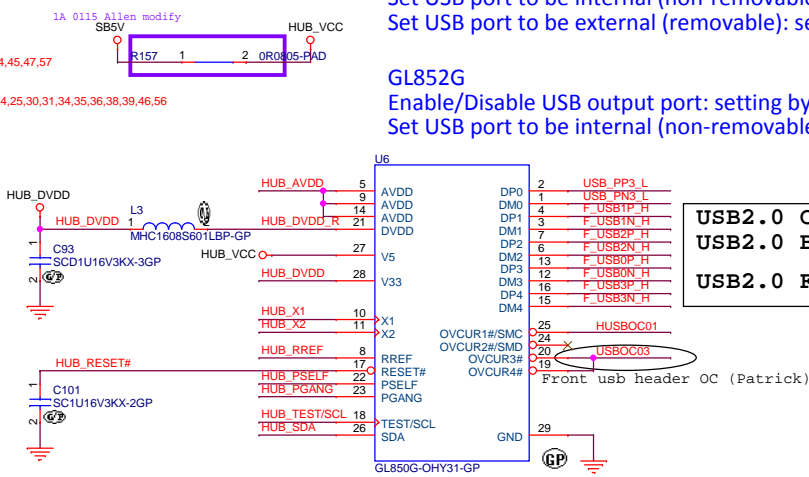
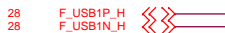
USB2.0 Front



USB2.0 BT



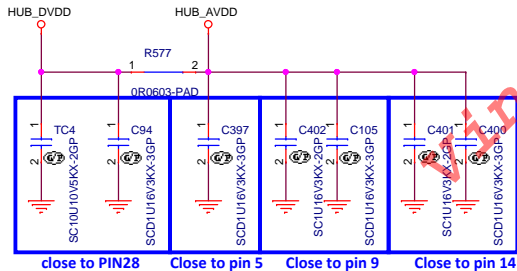
USB2.0 Card Reader



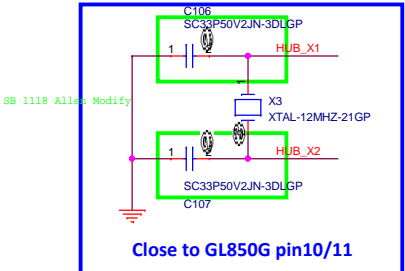
Co-lay GL850G and GL852G  
GL850G: 71.0850G.003 (USB2.0 STT 1 to 4)  
GL852G: 71.00852.A03 (USB2.0 MTT 1 to 4)

Internal Power

(Hub Internal VR output from pin 28 V33 = HUB\_DVDD)

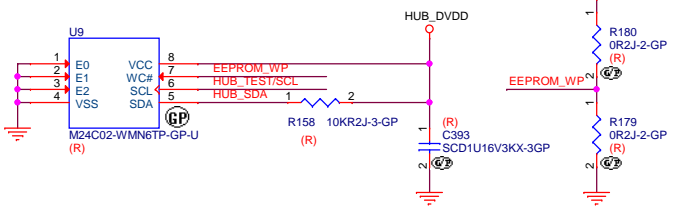


Xtal accuracy: +/- 20ppm



EEPROM

EEPROM is used for customized VID, PID, String, Configuration  
The purpose is to set 4 USB ports to be internal/external  
Default settings: 4 ports are external ports



V\_SP0\_A 30,31,40,46,47  
1DIV\_SS 12,15,17,20,23,30,34,38,40,46,57

## USB2.0 HUB

27 F\_USBPH\_H  
27 F\_USBIN\_H  
28,30,46 USB\_EN  
27 F\_USBP\_H  
27 F\_USBN\_H  
27 F\_USBP\_H  
27 F\_USBN\_H  
27 HUSB001

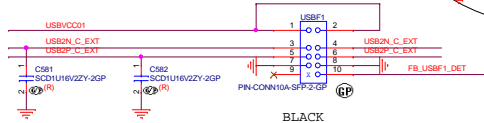
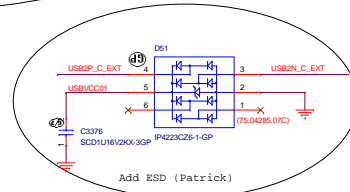
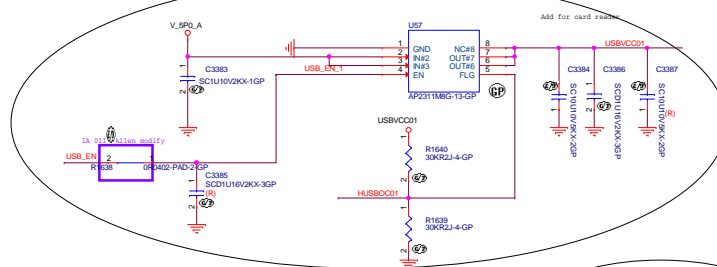
## USB 3.0

13 F\_USBP  
13 F\_USBN  
13 USB002  
13 USB30\_TXP0  
13 USB30\_TXN0  
13 USB30\_RXP0  
13 USB30\_RXN0

## USB HUB

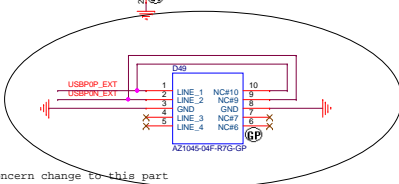
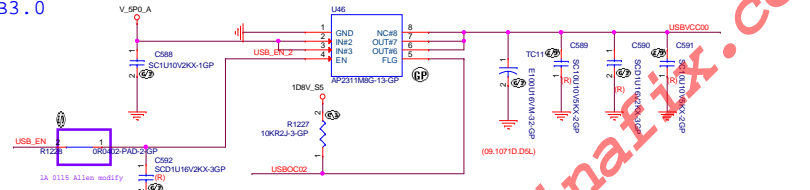
12 FB\_USBP\_DET  
12 FB\_USBN\_DET

## USB\_Power

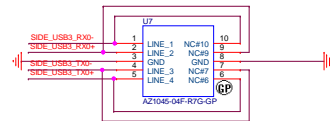


BLACK  
For Card Reader

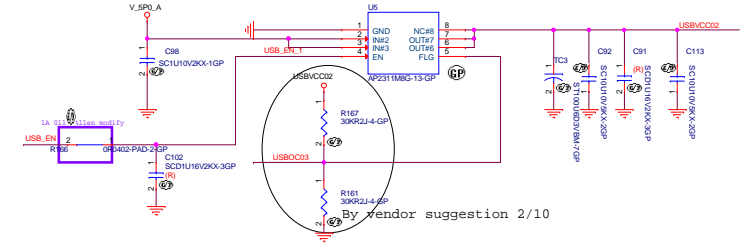
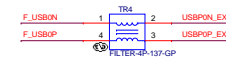
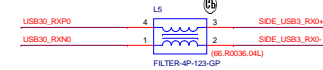
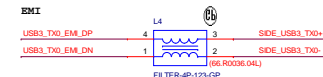
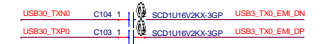
## USB3.0



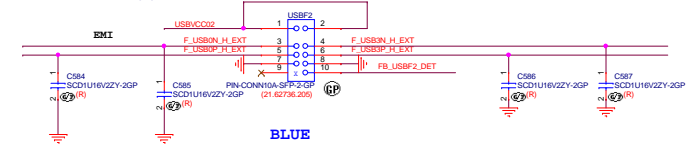
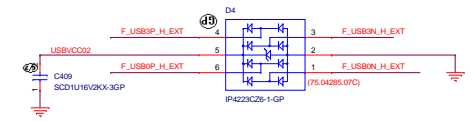
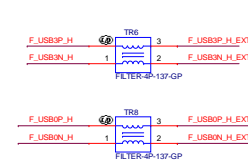
ITE concern change to this part



Vinalix.com

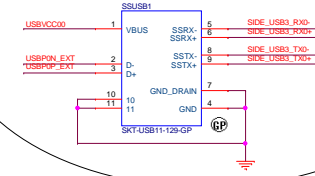


By vendor suggestion 2/10



BLUE  
For Front USB

## Side USB 3.0



<Variant Name>

Remove Card Reader

[vinafix.com](http://vinafix.com)

<Variant Name>

**wistron**

**Wistron Incorporated**  
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Hsichih, Taipei

Title  
NA

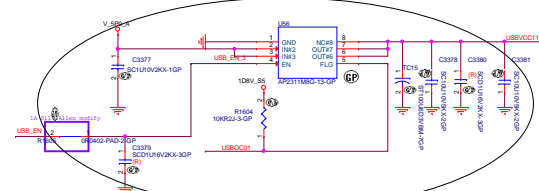
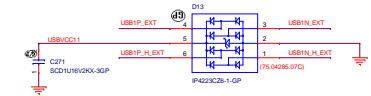
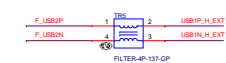
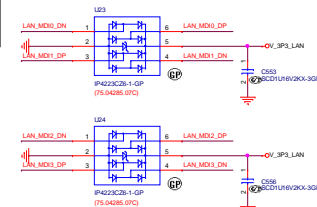
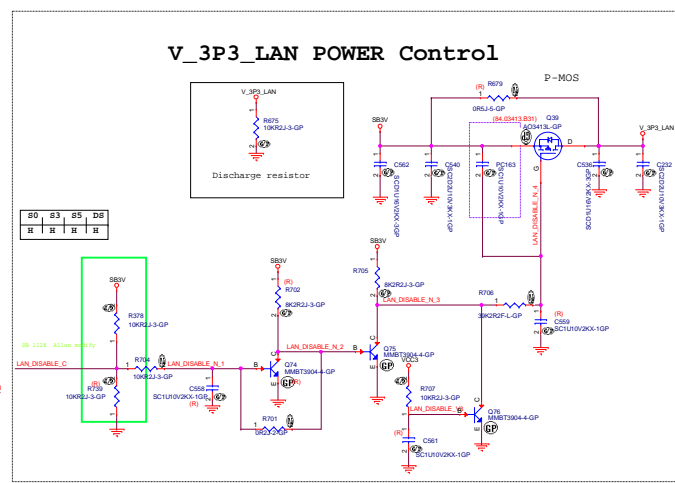
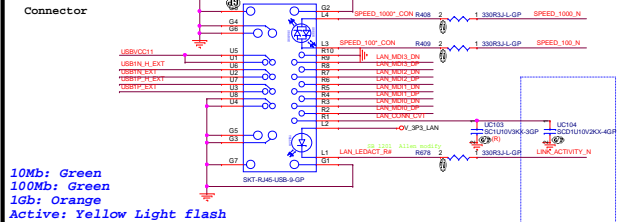
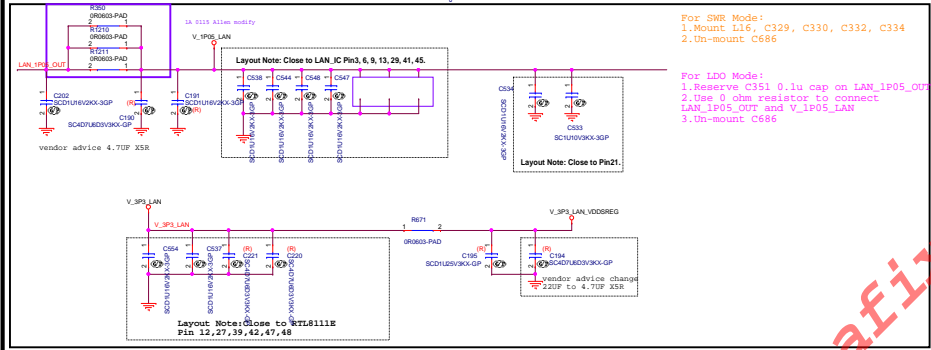
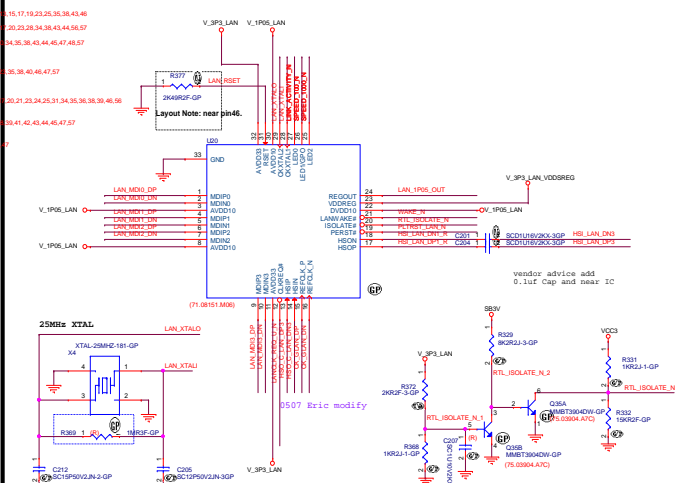
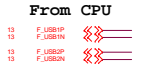
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B

Document Number  
Rosa\_BayTrail\_DT

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A00

Date: Tuesday, April 15, 2014

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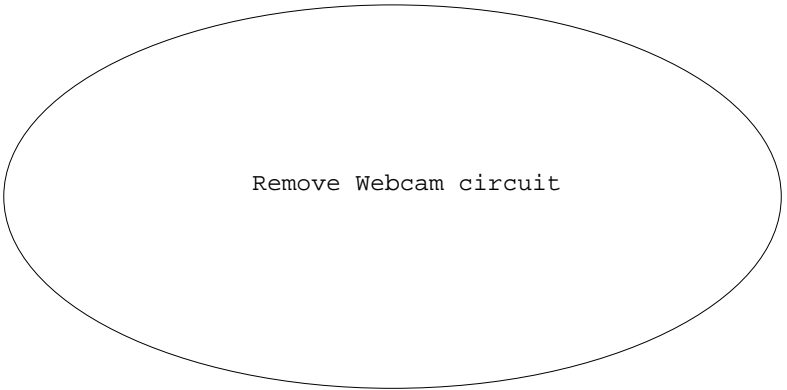




Remove AMP circuit

Vinafix.com





Remove Webcam circuit

[vinafix.com](http://vinafix.com)

Rev	A00
-----	-----

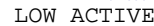
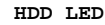
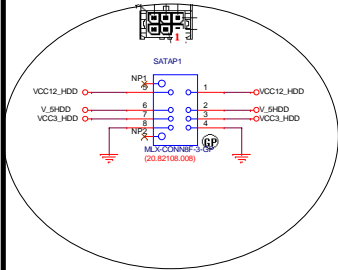


```
Pin1(VCC12)
```



12,23,38      PWRBTN\_N      << PWRBTN\_N

HD\_LED

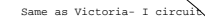


Black



Blue color

Blue



GP	LED_YELLOW	LED_GREEN
ORANGE (SUS_LED)	L	H
WHITE (PWR_LED)	H	L

File **SATA/LED/BTN**[illegible]

Size	Document Number
Custom	Rosa_BayTrail_DT

Date: Tuesday, April 15, 2014

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Hsichih, Taipei

Rev

ADD

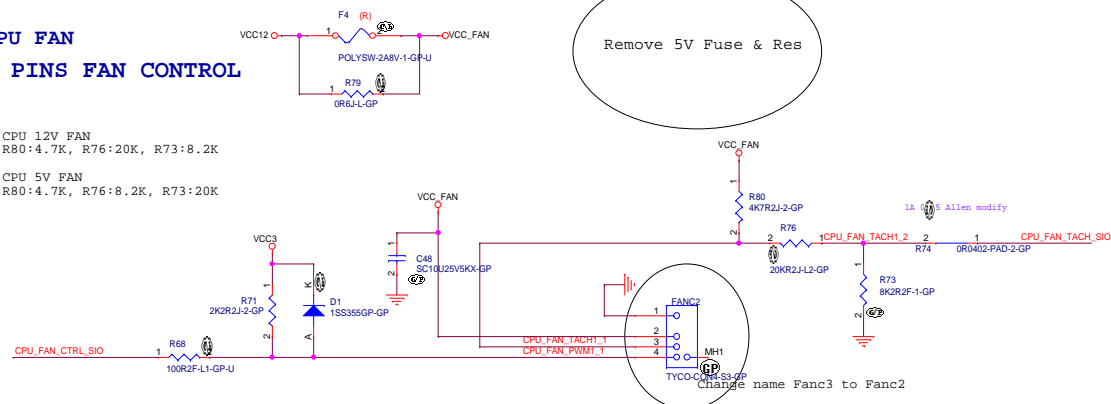
VCC3 <<< VCC3 12,13,15,17,20,21,23,24,25,30,31,34,35,36,39,46,56  
 VCC12 <<< VCC12 35,38,41

## CPU FAN 4 PINS FAN CONTROL

CPU 12V FAN  
 R80:4.7K, R76:20K, R73:8.2K  
 CPU 5V FAN  
 R80:4.7K, R76:8.2K, R73:20K

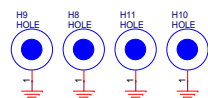
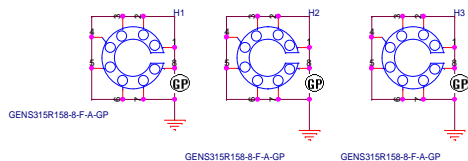
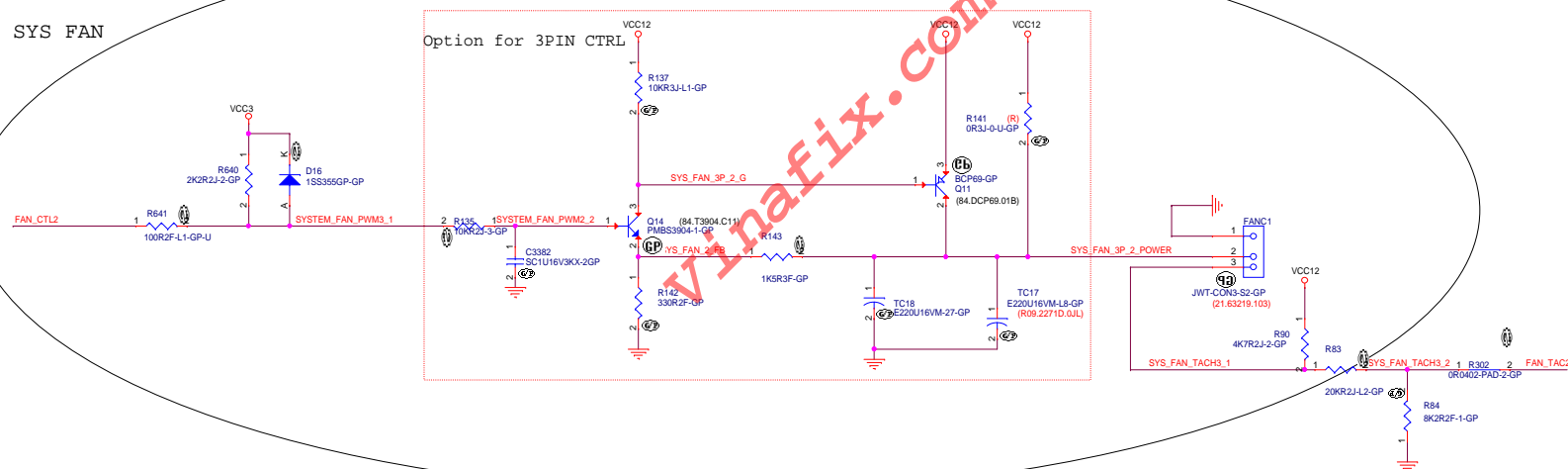
## SIO FAN CONTROL

38 CPU\_FAN\_CTRL\_SIO <<<  
 38 CPU\_FAN\_TACH\_SIO <<<  
 38 FAN\_TAC2 <<<  
 38 FAN\_CTL2 <<<

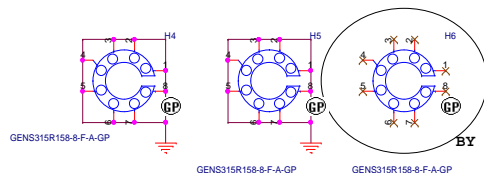


Change sys fan circuit same as Great Bear circuit and fan conn (Patrick)

## SYS FAN



CPU Heatsink screw hole.



BY vendor 不接任何gnd, 以防noise cover audio

<Variant Name>


**wistron**  
 FAN CIRCUITS/HOLE

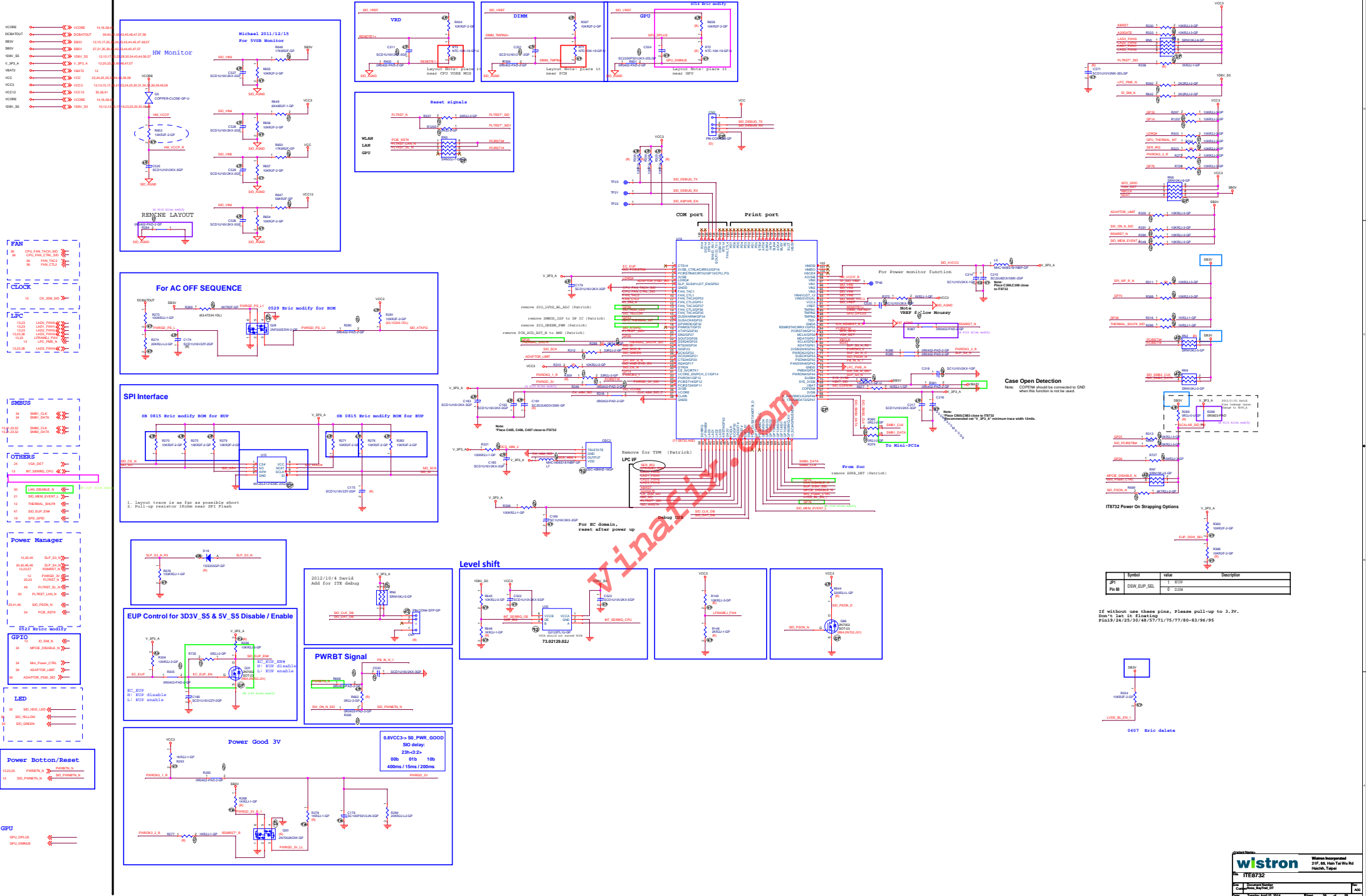
Wistron Incorporated  
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 Hsichih, Taipei

Size C Document Number Rosa\_BayTrail\_DT Rev A00  
 Date: Tuesday, April 15, 2014 Sheet 36 of 58

Remove TPM Function

Vinafix.com

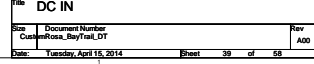
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		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title TPM			
Size	Document Number		Rev
CustomRose_BayTrail_DT			A00
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Symbol	value	Description
J1	DSW_EUP_SEL	1 STOP
Pin 10	0	DSW

If without use these pins, Please pull-up to 3.3V.  
Don't let it floating  
Pin19/24/25/30/48/57/71/75/77/80-83/96/99

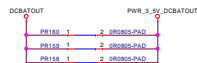




DCBATOUT 38.30,41.42,43,45,46,47,57,58

V\_3PS\_A 13.20,23,25,30,46,47,57

V\_5PS\_A 26,30,31,46,47

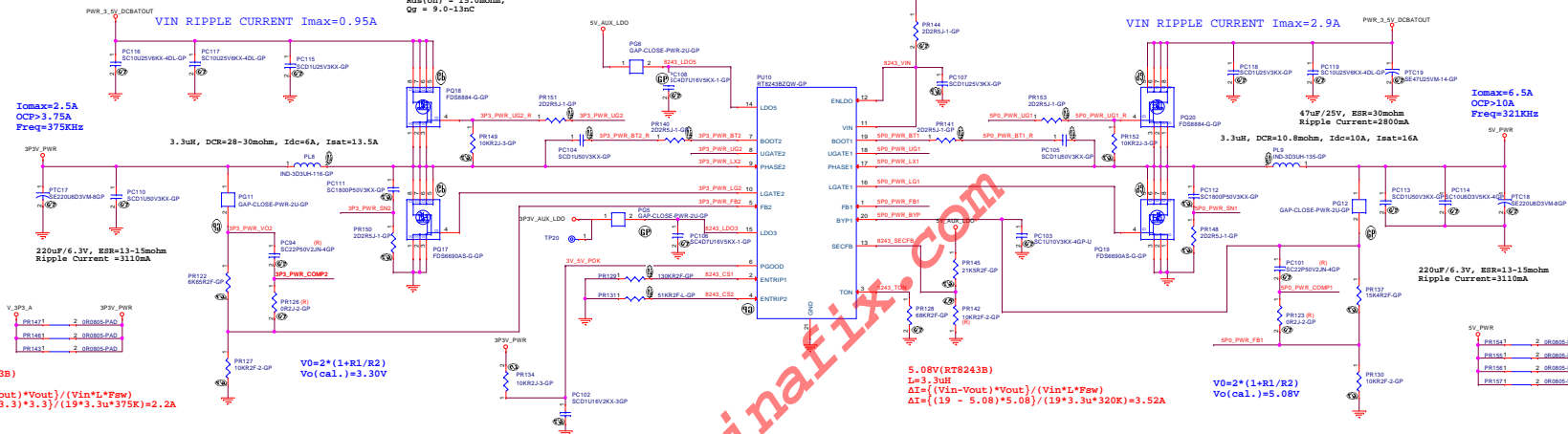


UG-84.08884.B37 FDS8884  
 $V_{gs} = 4.5V$ ,  
 $I_d = 7.5A$ ,  
 $R_{ds(on)} = 30.0m\Omega$ ,  
 $Q_g = 5.0-7.0nC$

LQ-84.06690.G37 FDS6690AS  
 $V_{gs} = 4.5V$ ,  
 $I_d = 10A$ ,  
 $R_{ds(on)} = 15.0m\Omega$ ,  
 $Q_g = 9.0-13nC$

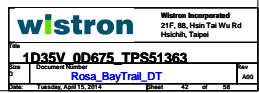
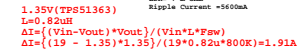
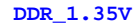
UG-84.08884.B37 FDS8884  
 $V_{gs} = 4.5V$ ,  
 $I_d = 7.5A$ ,  
 $R_{ds(on)} = 30.0m\Omega$ ,  
 $Q_g = 5.0-7.0nC$

LQ-84.06690.G37 FDS6690AS  
 $V_{gs} = 4.5V$ ,  
 $I_d = 10A$ ,  
 $R_{ds(on)} = 15.0m\Omega$ ,  
 $Q_g = 9.0-13nC$



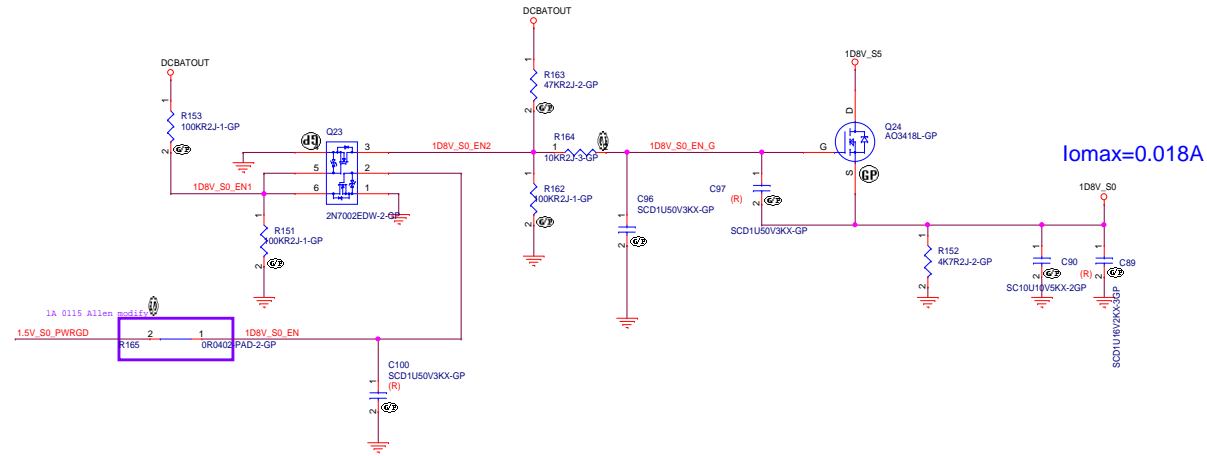




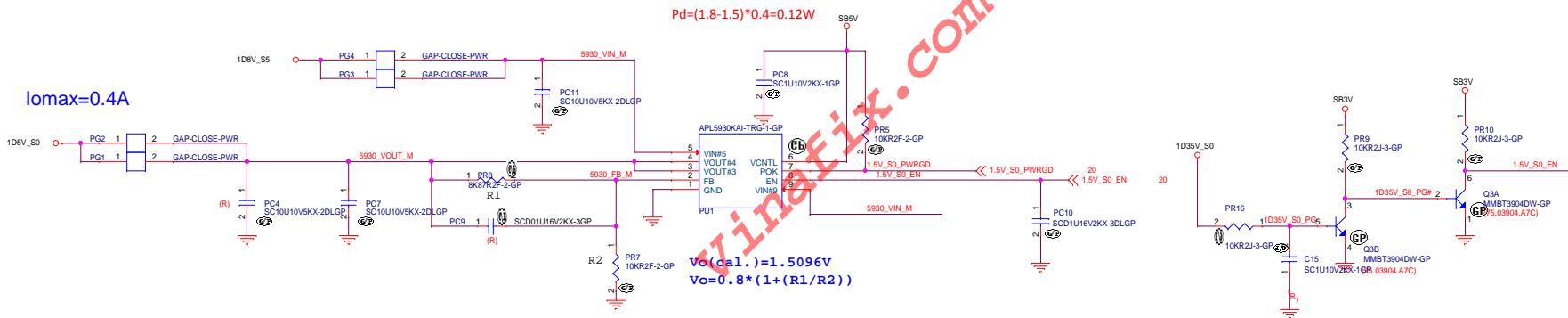


1D0V_S0	1D0V_S0	12,15,17,44,45
1D05V_S0	1D05V_S0	15,17
1D8V_S0	1D8V_S0	10,12,13,15,17,19,23,25,30,35,38,46
1D8V_S5	1D8V_S5	12,15,17,20,23,28,30,34,38,44,56,57
1D35V_S0	1D35V_S0	15,17,42
DCBATOUT	DCBATOUT	38,39,40,41,42,45,46,47,57,58
SB3V	SB3V	12,15,17,20,30,34,35,38,44,45,47,57
SB5V	SB5V	27,31,35,38,39,41,42,44,45,47,57
1D5V_S0	1D5V_S0	15,17,31,34

## 1.8V\_S0

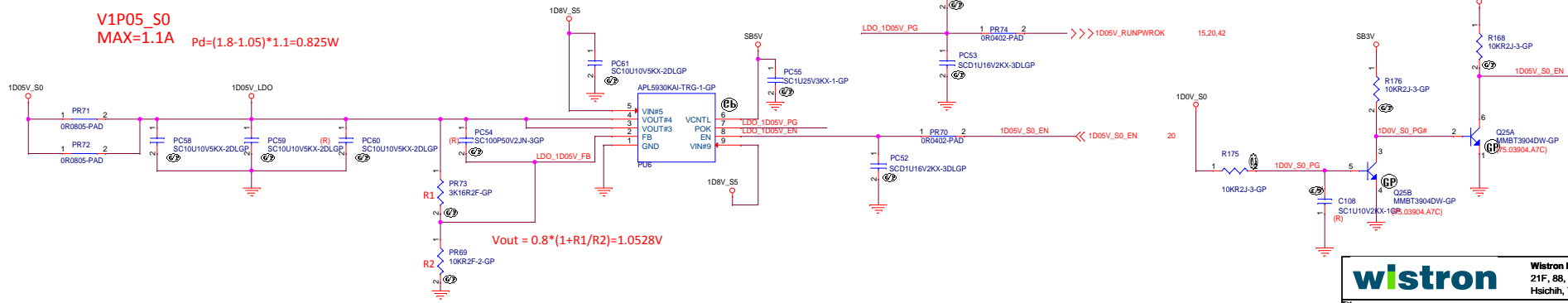


## 1.5V\_S0

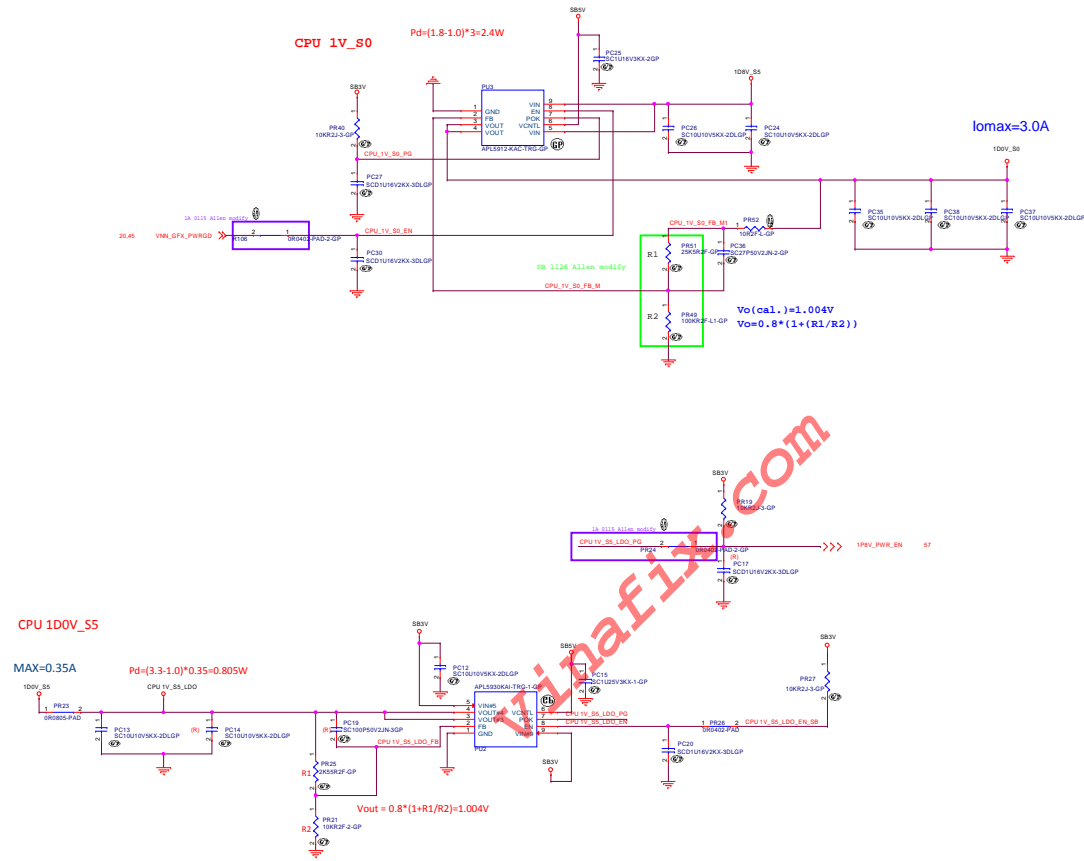


## V1P05\_S0 MAX=1.1A

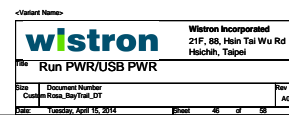
$$Pd=(1.8-1.05)*1.1=0.825W$$



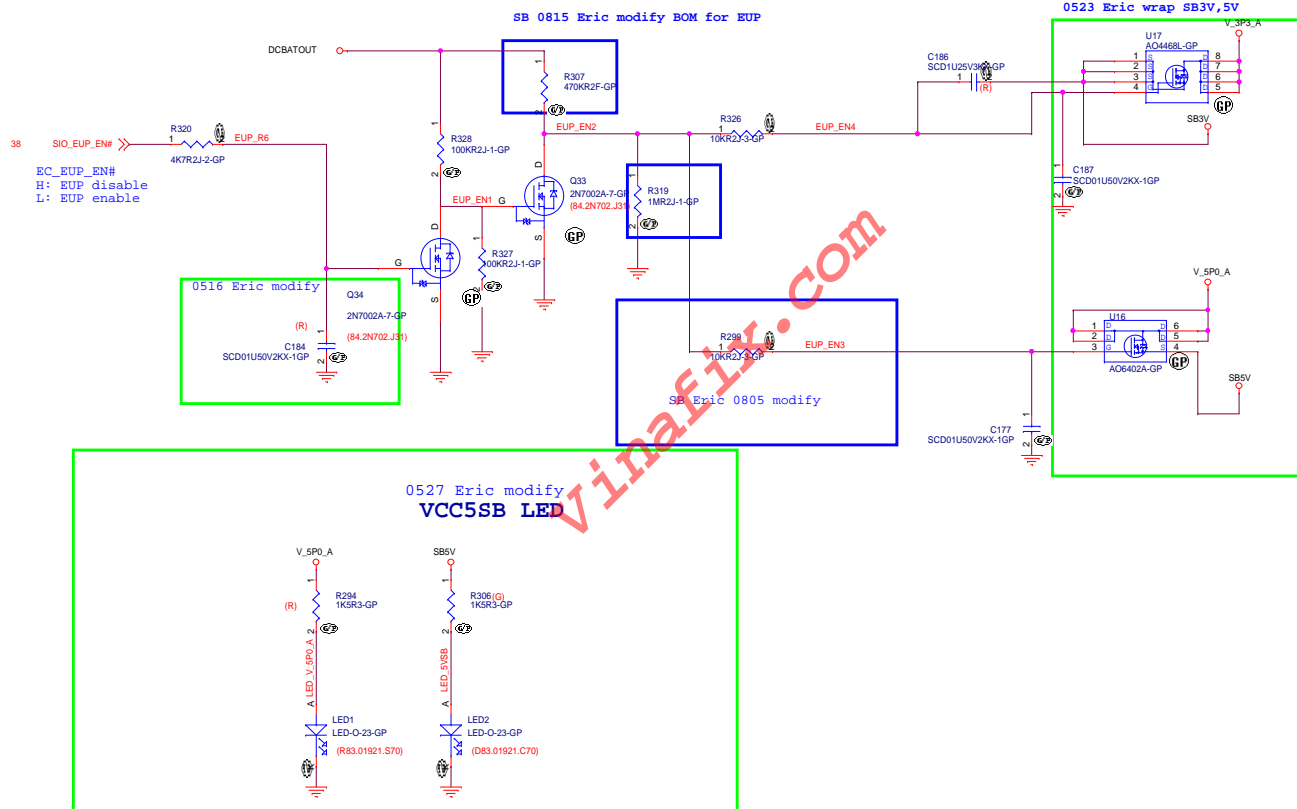
100V_S0	100V_S0	12,15,17,43,45
100V_S5	100V_S5	15,17
100V_S5	100V_S5	12,15,17,20,23,28,30,34,38,43,46,57
SB3V	SB3V	12,15,17,20,23,28,34,38,38,43,45,47,48,57
SB5V	SB5V	27,31,35,38,39,47,42,45,46,47,57






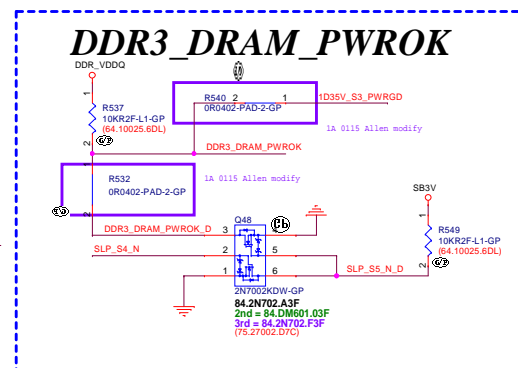


DCBATOUT	38,39,40,41,42,43,45,46,57,58
SB3V	12,15,17,20,30,34,35,38,43,44,45,48,57
SB5V	27,31,35,38,39,41,42,43,44,45,57
V_3P3_A	12,20,23,35,38,40,46,57
V_5P0_A	28,30,31,40,46



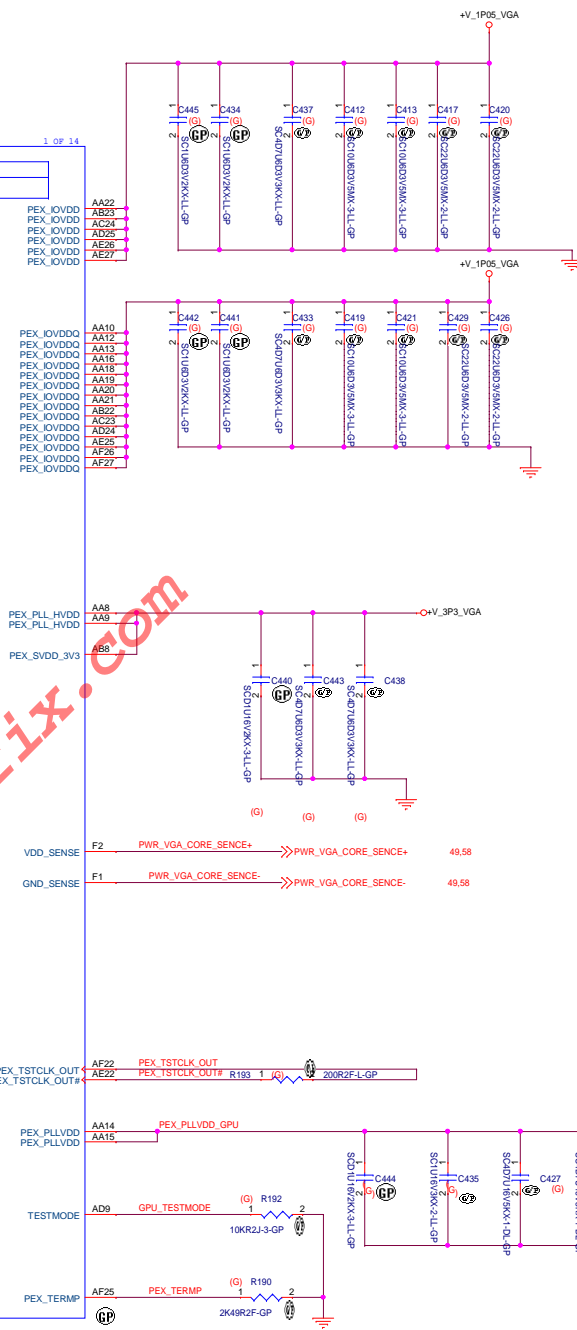
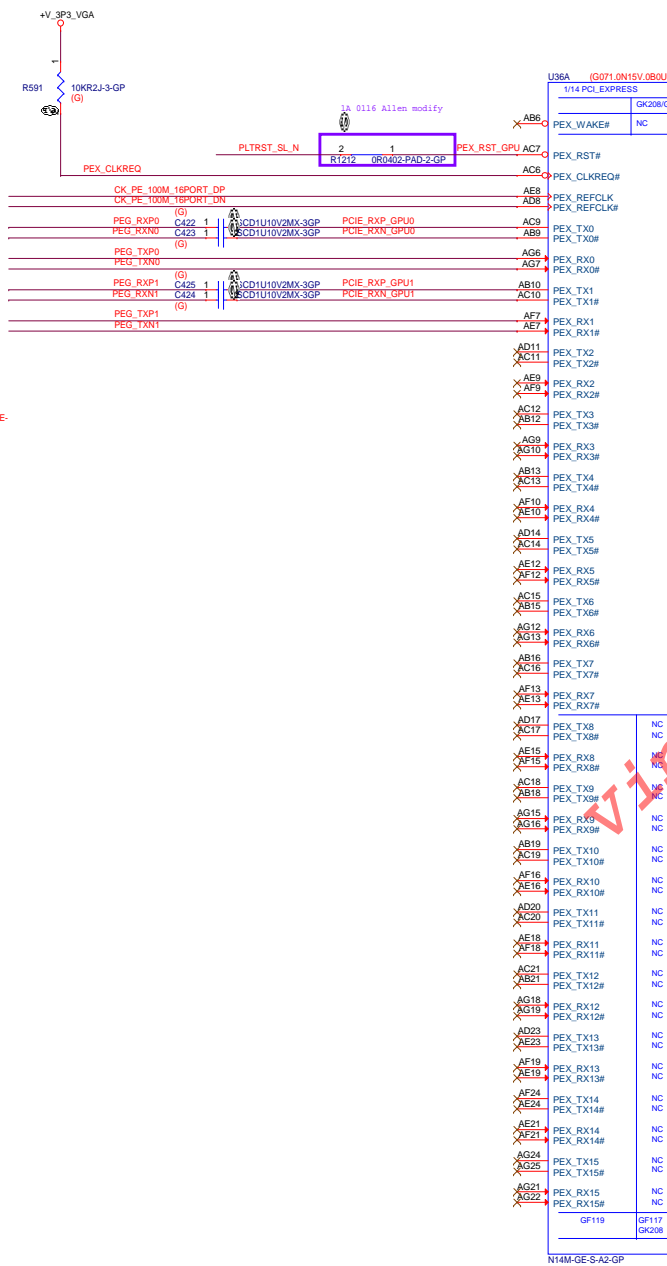
<Variant Name>

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
File PCH_1D05V			
Size C	Document Number Rosa_BayTrail_DT		Rev A00
Date:	Tuesday, April 15, 2014	Sheet 47 of 58	

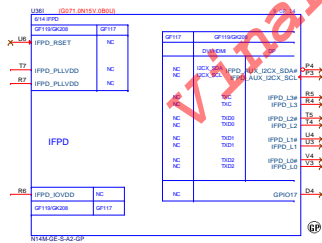
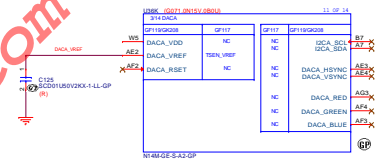
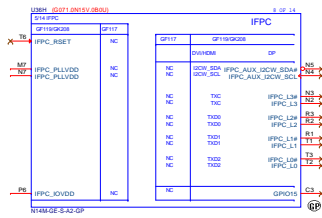
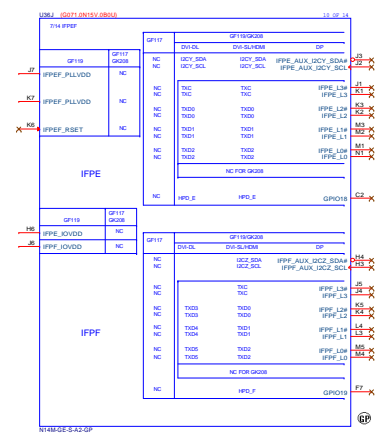
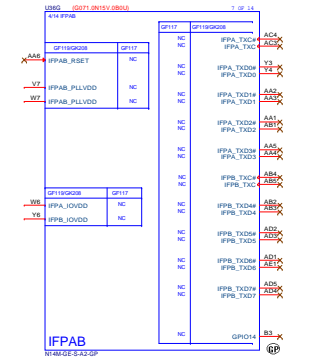


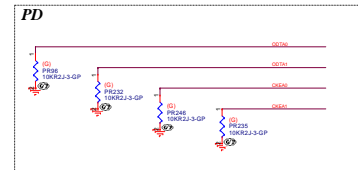
[vinafix.com](http://vinafix.com)





Add two 1uF Caps according to the NV Comment





OFFICE SCORE CARD MAPPING		
C000	931	33-63
C001	C007	
C002	C007	
C003	C007	
C004	934	A14
C005	937	K07
C006	96	96
C007	97	
C008	A2	
C009	90	
C010	AA	AA
C011	A1	A1
C012	BA	BA
C013	907	907
C014	A15	A15
C015	C007	C007
C016	C007	C007
C017		
C018	C008	C008
C019		
C020	933	96
C021	96	96
C022	911	911
C023	96	96
C024	93	93
C025	BA2	BA2
C026	932	932
C027	9407	9407
C028	935	935
C029	9407	9407
C030		

- **IDEs not required for any of 8 iterations, even up to 6GB density**
- **IDEs only needed if we support 8 configurations, not only at 6GB**

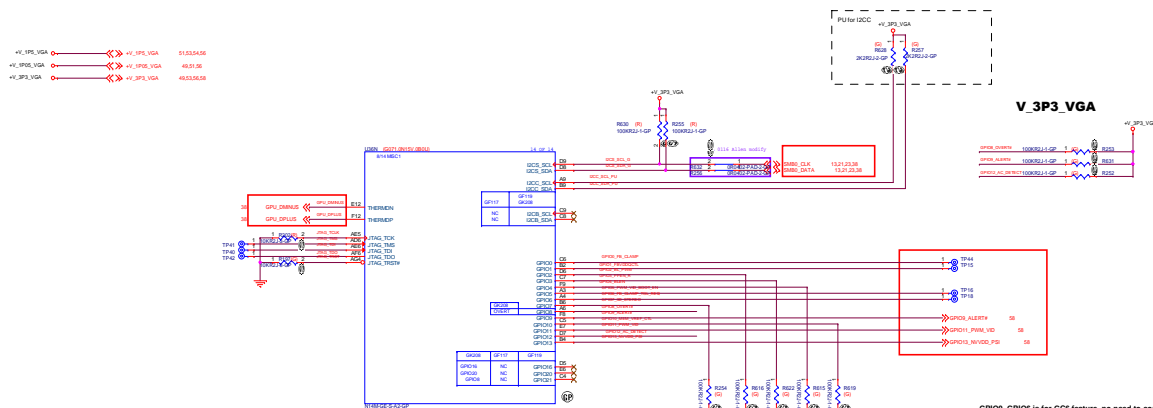


Table 115. G82-64 and GB4-128 GPIO Description

- GPIO20 and GPIO21 are only available on H14M-LP/-GS/-HE/-HS & H14P-GV/-GV2
- The greyed out section of Table 107 indicates GPIOs that are not available for H14M-GS/GV2

GPIO0, GPIO6 is for GC6 feature, no need to connect since this project won't support GC6.  
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-States.  
GPIO12 : High->AC Mode,Low->Battery Mode enter slow down functionpull for power saving.Recommand:Pull-High for AC mode  
GPIO13 PSI :Change Phase from two to one, and then enter slow down functionpull for power saving.

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M16 DDR3	Alcon	0x1	1.5 V 1.5 V	MT41J128M16JT- 093GK	1000	1150	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	MT41J128M16J1T- 107GK	900	1150	Production Candidate
				K4V2G1646E-BC1A	1000	1204	Production Candidate
				K4V2G1646E-BC11	900	1204	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-10C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration 256M 16 D0R3	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
	Samsung	0x0	1.5 V/ 1.5 V	K4W46-16A68-11C1	900	N/A	Production Candidate
	Micron	0x0	1.5 V/ 1.5 V	MT41K256M16HA- 107G-E	900	N/A	Production Candidate
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63AFR-11C	900	N/A	Production Candidate
		0x4		H5TQ4G63AFR-11C		N/A	Post-Production Candidate

## STRAP

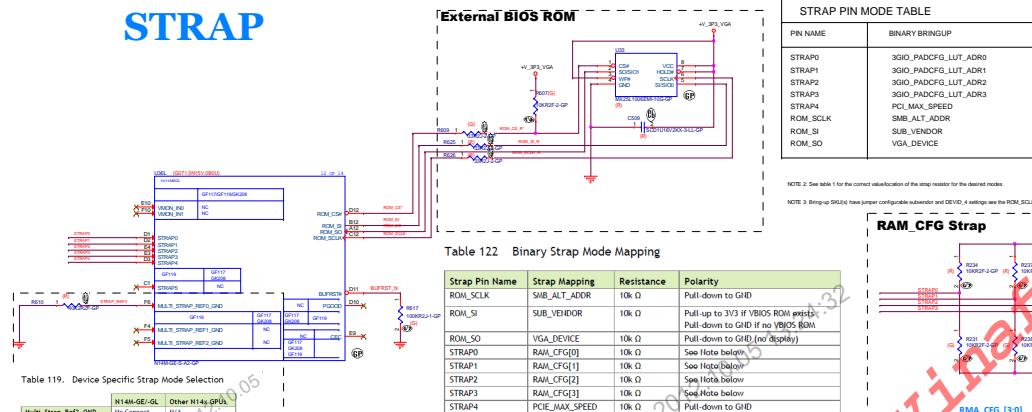
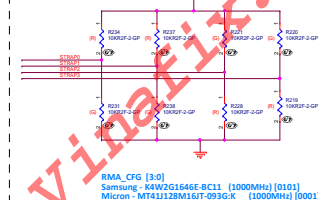


Table 122 Binary Strap Mode Mapping

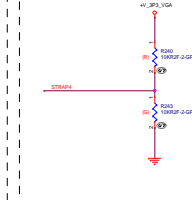
Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCL	SMB_ALERT	10k $\Omega$	Pull-down to GND
ROM_SI	SMB_VENDOR		
			Pull-up to V3V3 if YB05 ROM present; Pull-down to GND if no YB05 ROM.
ROM_S0	VGA_DEVICE	10k $\Omega$	
STRAP0	RA0L_CFG0	10k $\Omega$	Pull-down to GND (no display)
STRAP1	RA0L_CFG1	10k $\Omega$	See Note below
STRAP2	RA0L_CFG2	10k $\Omega$	See Note below
STRAP3	RA0L_CFG3	10k $\Omega$	See Note below
STRAP4	POE_MAX_SPEED	10k $\Omega$	Pull-down to GND

Refer to the latest version of H14M-GE/ GL *Memory Recommended Vendor List* for the specific setting for each memory type and configuration. Pull-up to 3V3 for binary '1' and pull-down to GND for binary '0'.

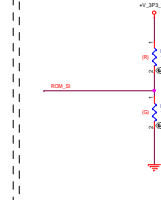
**RAM\_CFG Strap**



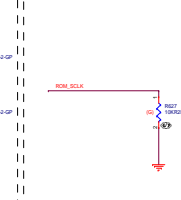
## PCIE\_MAX\_SPEED Strap



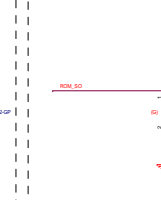
**SUB\_VENDOR Strap**



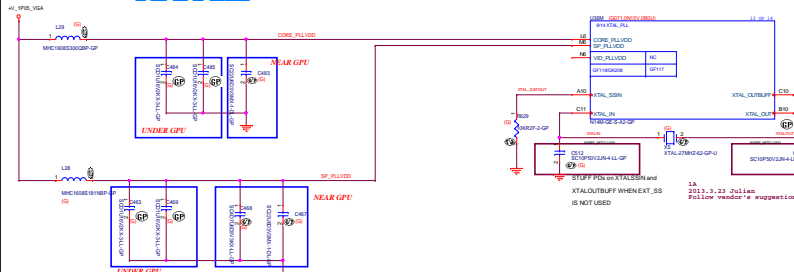
**SMB\_ALT\_ADDR Strap**



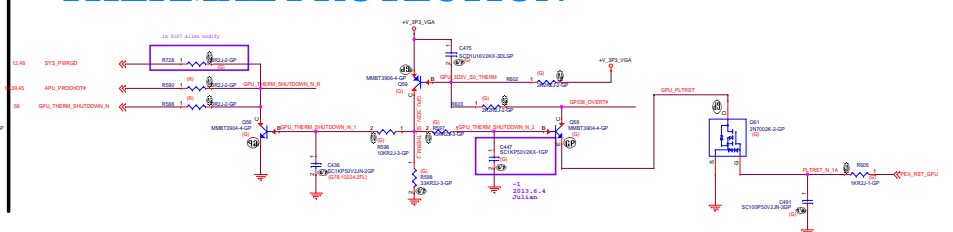
### VGA\_DEVICE Strap



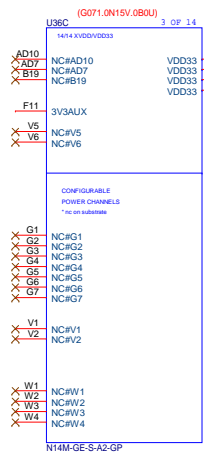
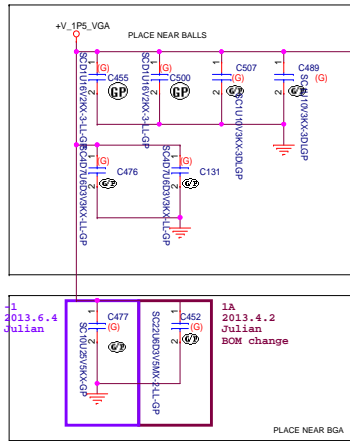
## XTAL



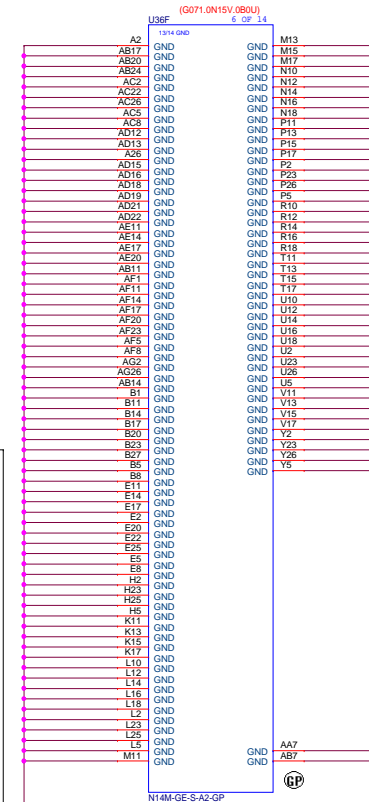
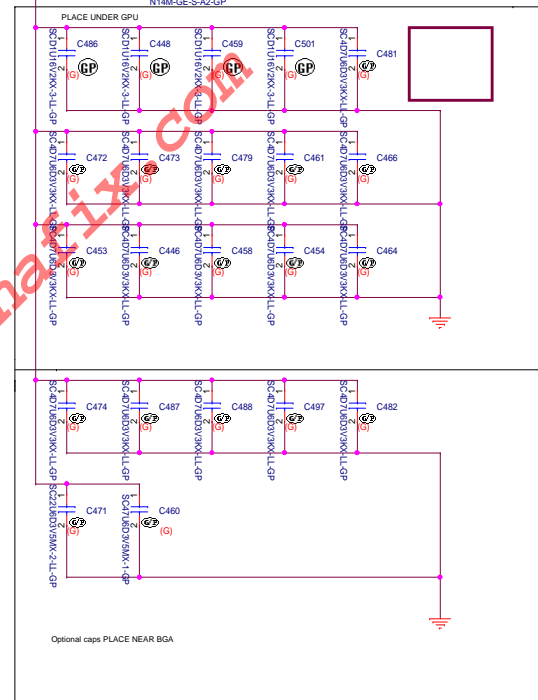
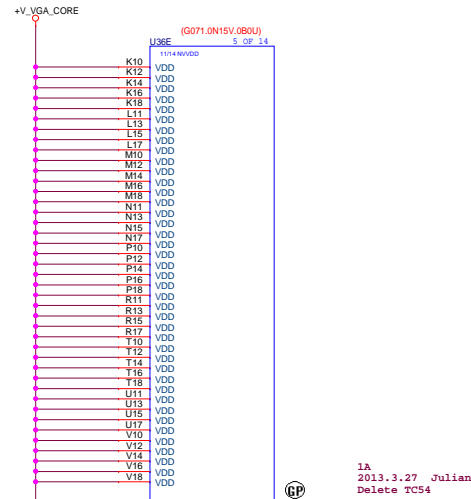
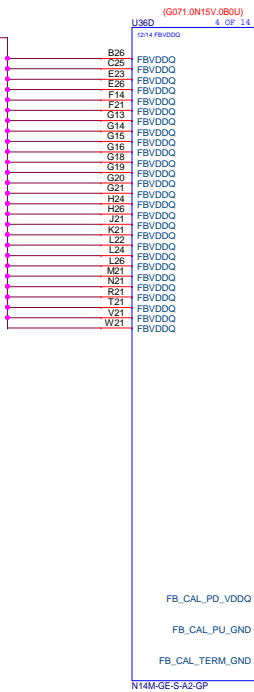
## THERMAL PROTECTION



+V\_1P05\_VGA <<>> +V\_1P05\_VGA 49,51,52,56  
 +V\_1P5\_VGA <<>> +V\_1P5\_VGA 51,54,56  
 +V\_3P3\_VGA <<>> +V\_3P3\_VGA 49,52,56,58  
 +V\_VGA\_CORE <<>> +V\_VGA\_CORE 58



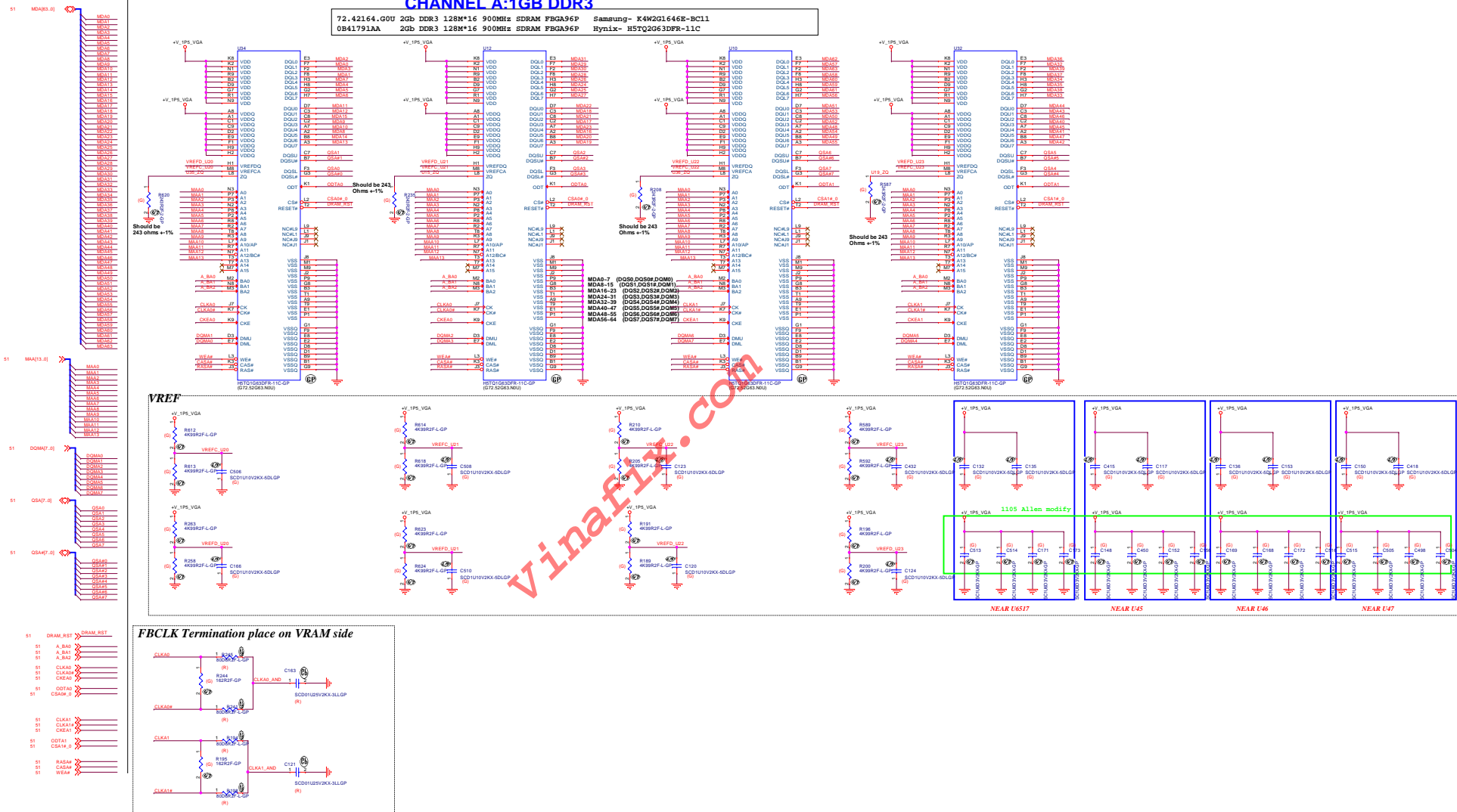
\*\* XPWR pins are configurable.  
 These pins are not connected on the substrate.  
 Therefore, XPWR pins can be assigned as needed,  
 to improve Top layer routing, power delivery.



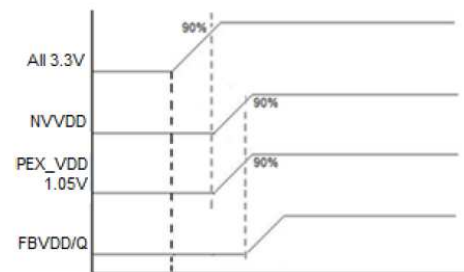
AV\_1PS\_VGA 0 4V\_1PS\_VGA 51.53.56  
AV\_1PS\_VGA 0 4V\_1PS\_VGA 48.51.52.56

## CHANNEL A:1GB DDR3

72.42164.G0U 2Gb DDR3 128M\*16 900MHz SDRAM FBGA96P Samsung K4W2G1646E-BC11  
0B41791AA 2Gb DDR3 128M\*16 900MHz SDRAM FBGA96P Hynix H5TQ2G63DFR-11C



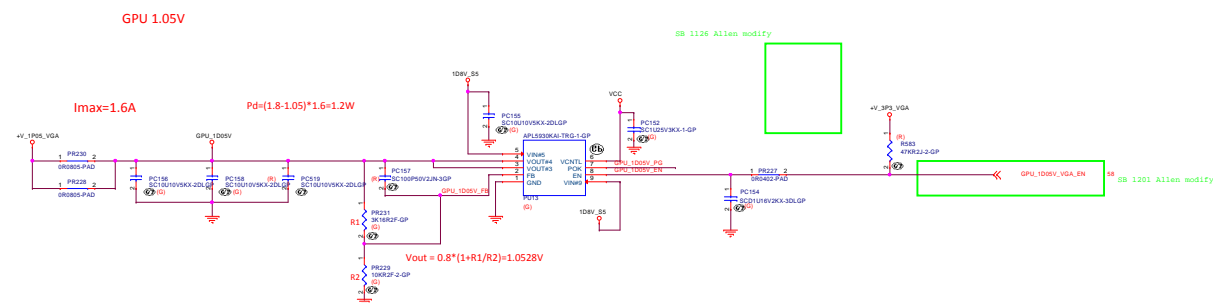
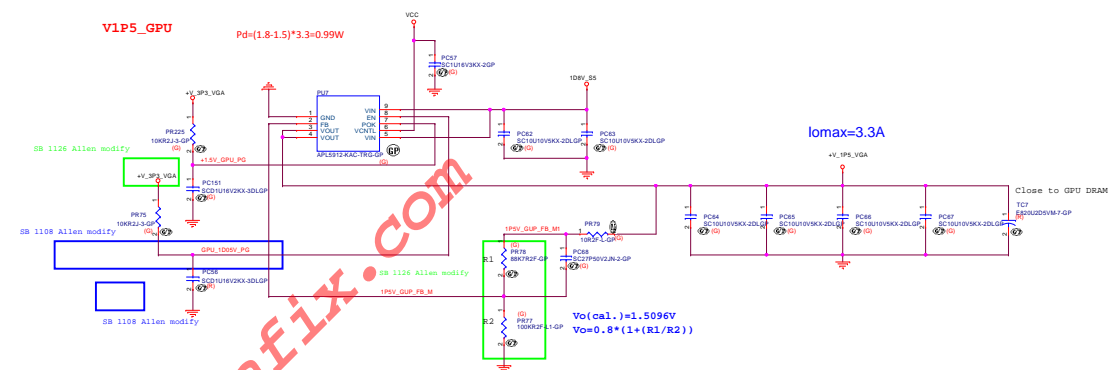
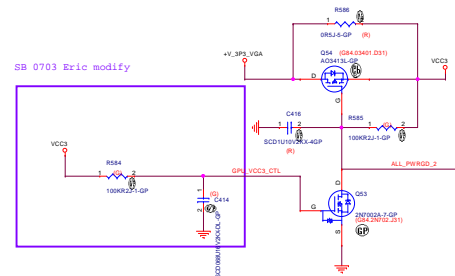
3.3V-->NVVDD&PEX\_VDD(+V\_VGA\_CORE&+V\_1P05\_VGA)-->FBVDD/Q(+V\_1P5\_VGA)



Notes: - All 3.3V includes all rails powered at 3.3V  
- PEX\_VDD 1.05V includes all rails that are shared

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### 3D3V\_S0 to 3D3V\_DELAY Transfer





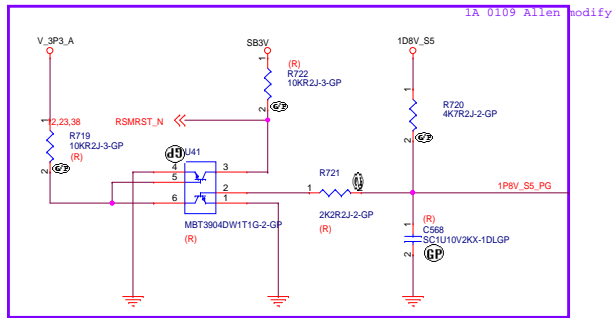
1D8V\_S5 <<> 1D8V\_S5 12,15,17,20,23,28,30,34,38,43,44,56

DCBATOUT <<> DCBATOUT 38,39,40,41,42,43,45,46,47,58

SB3V <<> SB3V 12,15,17,20,30,34,35,38,43,44,45,47,48

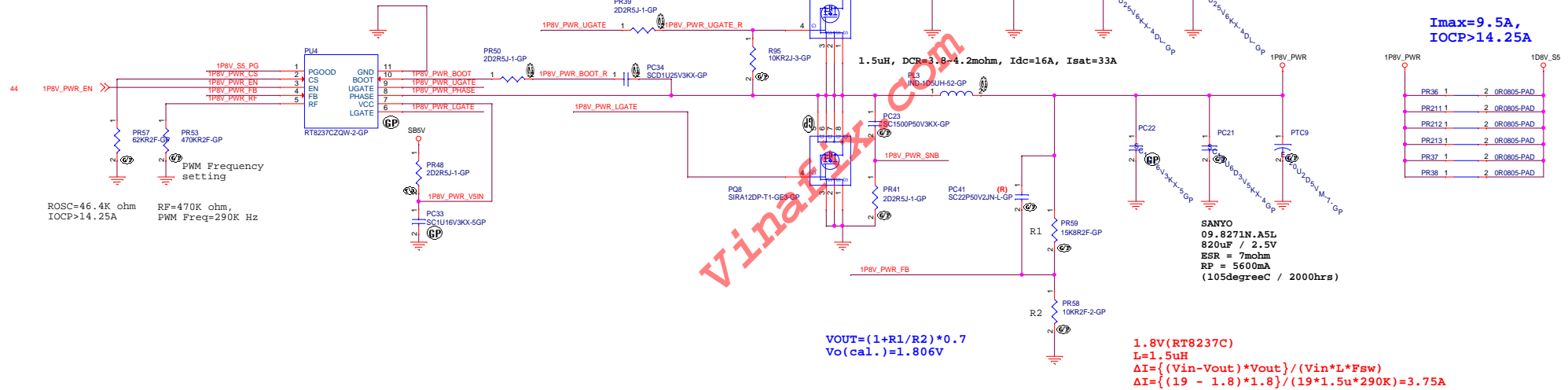
SB5V <<> SB5V 27,31,35,38,39,41,42,43,44,45,47

V\_3P3\_A <<> V\_3P3\_A 12,20,23,35,38,40,46,47



84.00172.A37 SIR172ADP  
Vgs @ 4.5V,  
Id = 12.9A,  
Rds(on) = 8.5-10.5mohm,

84.SRA12.037 SIRA12DP  
Vgs @ 4.5V,  
Id = 20A,  
Rds(on) = 4.4-6.0mohm,



+V\_3P3\_VGA 49.52,53.56  
 +V\_VGA\_CORE 53  
 DCBATOUT 38.39,40,41,42,43,45,46,47,57  
 VCC 23,24,25,38,39,42,48,56

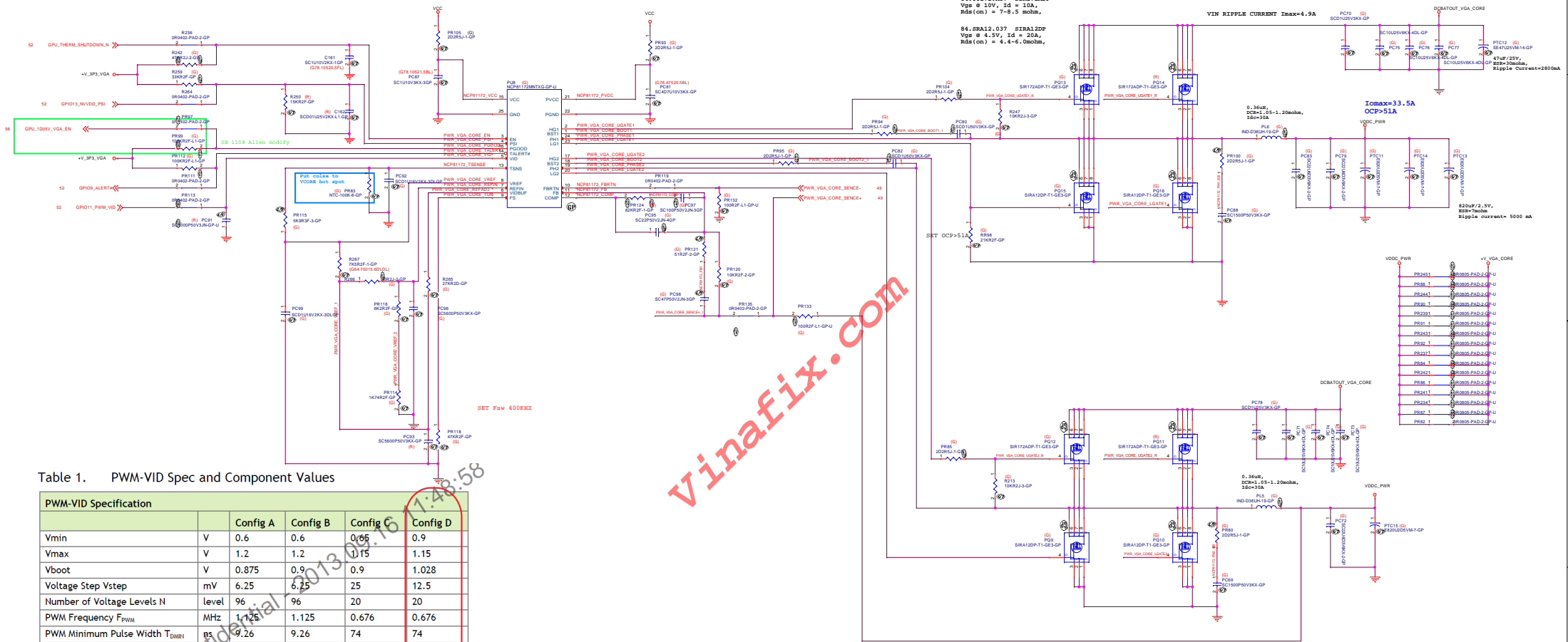


Table 1. PWM-VID Spec and Component Values

PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency $F_{PWM}$	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width $T_{DMH}$	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	K $\Omega$	39	20	39	27
R2 (1%)	K $\Omega$	39	20	30	7.5
R3 (1%)	K $\Omega$	1.5	2	3	0
R4 (1%)	K $\Omega$	30	18	24	6.2
R5 (1%)	K $\Omega$	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6